

PICMG ISA / PCI Passive Backplane

The PCI/ISA industrial PC standard allows integrators of passive-backplane systems based on PC architectures access to the performance of PCI-based peripheral controllers, while maintaining compatibility between processor cards from multiple manufacturers and enabling continued use of existing ISA-based I/O. This is an overview of the standard and the thinking behind it.

Introduction

The development of PCs based on passive backplane technology has been driven by the needs of the industrial and Computer-Telephony Integration (CTI) markets. PCs designed for desktop use are based on motherboard architectures which fail to address a number of important requirements for industrial and CTI use.

A motherboard structure is inflexible and may require the replacement of the entire motherboard in order to repair or to upgrade the system. This, in turn, results in long system downtime, which may be tolerable in a system used for office applications, but which is totally unacceptable in a system which controls the core processes on which a business depends.

Many industrial and CTI applications require a large number of expansion slots for real-world I/O or speech cards. These are not available on motherboard-based PCs, while the overall construction of the motherboard and I/O expansion board system is not designed to cope with the environmental demands of many industrial applications.

A passive-backplane architecture solves these problems by completely dispensing with the motherboard. In a passive backplane PC, a system bus is used to interconnect a plug-in processor board and multiple plug-in add-on boards. This architecture makes rapid repair by board substitution possible and system upgrades and changes are greatly simplified, with minimum resulting system downtime. There is considerable scope for system expansion, with up to 20 ISA slots available for I/O or speech cards. The rugged construction of a typical passive-backplane system provides reliable operation in an industrial environment.

PCI - An opportunity and a problem

While a passive backplane architecture solves the problems associated with the traditional motherboard architecture the rapidly increasing throughput of I/O systems presents new challenges. The data transfer requirements of fast disk sub-systems and high-speed networks are difficult to meet with an ISA or even a higher speed EISA I/O bus. At the same time, the Peripheral Comp-

onent Interconnect (PCI) has become a widely used element in high-

volume personal computers and single-board computer designs. With a 32-bit data path and a bandwidth of up to 133 Mbytes/sec, PCI offers the throughput demanded by the latest I/O and storage devices.

The PCI interface is processor independent, operating on its own clock rather than that of the processor devices. Computer boards based on X86, PowerPC and Alpha AXP processors use PCI as the local bus. The Alpha AXP microprocessor and many peripheral I/O controllers are already available with integral PCI interface. The widespread use of PCI brings economies of scale and resulting lower costs.

The specification of a passive backplane PC architecture using PCI raises issues of vendor interoperability and standards. A passive-backplane system based solely on the ISA bus standard can simply adopt the ISA board format for the processor board, ensuring compatibility between plug-in SBCs and backplanes from multiple vendors. However, no suitable standard existed for an implementation which would support existing ISA I/O cards and allow the use of PCI for high-performance channels. Areas which required definition were:

The mechanical form-factor of a plug-in single board computer. The mechanical form-factor of the passive backplane. The logical interface between the single board computer and the passive backplane. Backplane slot-specific signals and pin assignments

It was therefore necessary to generate a specification for the implementation of PCI on a passive backplane system. In order to deliver the benefits of vendor interoperability and economies of scale, an open standard under the control of an independent specifying body was required. However, at the time no suitable group existed.

The Solution - PICMG and the PCI/ISA Industrial Standard

A group of industrial computer product vendors, with a long history of developing PC architecture products for industrial and embedded control, were aware of the necessity for a configuration standard for PCI and joined forces. In May 1994 the PCI Industrial Computer Manufacturers Group (PICMG) was established with the mission to define an industrial PCI/ISA passive backplane and CPU card interface specification. The PICMG technical committee generated a comprehensive specification for a passive backplane architecture to support both PCI and ISA I/O buses.

The PCI/ISA industrial standard provides a broad-based open standard designed to maximize interoperability with other standards. Key objectives of the specification were:

- To enable interoperability between plug-in single-board computers and passive backplanes from different manufacturers.
- To ensure compatibility between passive backplanes built to the standard and off-the-shelf ISA and PCI adapters.
- To allow older technology ISA based SBCs to work in the new PCI/ISA backplanes.
- To allow an SBC with internal PCI bus to operate in an ISA-based system.
- To cater for upgrade to 64-bit PCI.

CPU/Backplane interface

The PCI/ISA industrial standard specifies the logical and mechanical interface between the CPU and the passive backplane. Instead of redesigning the entire edge connector on the CPU card, the PICMG technical committee decided to use a physical board format and connector based on the ISA adapter specification and add a PCI connector below, and in line with, the ISA connector, allowing sufficient space for 32-bit or 64-bit PCI interfaces.

The single-board computer can draw power from pins on the ISA connector and/or from pins on the PCI connector. This avoids the maximum power available to a CPU board being limited by the PCI local bus specification. The signals on the PCI interface have the same pin numbers as a PCI expansion slot with the following additions:

REQ# (3, 2, 1, 0)	Request signals for each PCI slot
GNT# (3, 2, 1, 0)	Grant signals for each PCI slot
CLKA	Clock for slot 1
CLKB	Clock for slot 2
CLKC	Clock for slot 3
CLKD	Clock for slot 4

The adoption of a standard ISA adapter board and connector format with additional PCI connector enables a two-stage approach to system upgrade. The first stage is to use a PCI-based single-board computer in an existing ISA passive-backplane system. This improves performance thanks to the faster internal bus on the processor board. The second stage is to replace the backplane or system chassis with a PCI industrial standard passive

backplane, when the additional performance will be extended to the PCI expansion bus.

PCI Expansion Bus

The specification defines backplane signals for up to four PCI bus slots which can be implemented as masters or slaves. A master slot has the additional REQ and GNT signals which enable a card to acquire control of the bus for transmission of data without central CPU intervention, making higher transfer speeds possible for SCSI controllers, fast Ethernet adapters and multi-media cards. Slave cards, such as modems, use the central CPU to move data. Some processor boards do not support masters in all four slots, since many PCI cards do not have a master capability.

Slot-specific signals

The PCI specification includes slot-specific signals which allow a processor to select specific slots and read configuration information during the boot process. This enables the processor to determine the identity of the PCI board in each slot and to configure the system accordingly, dispensing with the need for the system integrator to change jumpers or switches. The relationship between the select signals (IDSEL) and the allocation of the interrupt signals on the backplane must be known to the CPU board BIOS. The PICMG specification requires address/data bit 31 (AD31) to be routed to IDSEL on slot 1 (the PCI slot next to the PCI/ISA processor slot), AD30 to slot 2, AD29 to slot 3 and AD28 to slot 4. The pin assignment of REQ, GNT CLK and IDSEL signals for each PCI slot is shown in figure 3.

Interrupt signal assignment

The relationship between the IDSEL signals and interrupt lines for each slot are defined as part of the PICMG specification. This enables the BIOS configuration program to be standardized and takes full advantage of the four interrupt lines defined by the PCI specification. The layout used will facilitate the implementation of a PCI to PCI bridge on passive backplane systems. The interrupt signal assignment to each PCI slot is shown in figure 4.

Implementation examples

PICMG members have designed families of dual architecture PCI/ISA systems which meet the PCI/ISA industrial specification. These offer the system integrator the best of both worlds. The ISA bus offers full backwards compatibility with existing PC hardware and software while PCI provides the bandwidth necessary to take full advantage of the latest fast peripherals and high-speed networks. Backplanes with a dual-bus CPU connector, 1 to 4 PCI connectors and 6, to 15 ISA connectors are available.

The dual-bus architecture has proved to be very popular for voice applications. The ISA bus provides full back

ward compatibility with existing ISA-based speech telephony cards, while PCI provides access to the latest high-bandwidth disk I/O and networking sub-systems. Telephony systems based on traditional PC platforms often suffer from disk I/O bottlenecks, due to the limited capacity of the ISA bus with its 8 Mbytes/sec data rate and standard 10 Mbps Ethernet can reach saturation with just a few systems on the network. By eliminating the bottlenecks inherent in traditional PC implementations of Voice systems, the new architecture can boost system throughput by an order of magnitude.