NOTE: This short form specification is a subset of the CompactPCI Packet Switching Backplane specification, PICMG 2.16 R 1.0. For complete guidelines on the design of CompactPCI Packet Switching Backplane implementations, the full specification is required.

For a full copy of the PICMG 2.16 specification, go to www.picmg.org, or contact the PCI Industrial Computer Manufacturers Group at 401 Edgewater Place, Suite 500, Wakefield, Mass., 01880. Phone 781-246-9318, fax 781-224-1239, email info@picmg.org.

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INTRODUCTION

Ethernet network technology continues to be incorporated into more products than ever before. Once networked, components are relatively easy to integrate, allowing acceleration of system development.

Existing network technology is naturally bridged by networked components, thus providing unparalleled system scalability. The continued ability of products to interoperate is essential to the timely development and evolution of systems in a changing world. Opportunities remain for improving the rapid integration of products that will continue to adapt to the special needs of the industry.

The CompactPCI Packet Switching Backplane (CompactPCI/PSB) is an extension to the PICMG 2.x family of specifications that overlays a packet-based switching architecture on top of CompactPCI to create an Embedded System Area Network (ESAN). It supplements the robust, reliable and hot-swap capable CompactPCI architecture with the easily integrated, low-cost, high-performance, and extensible Ethernet. This creates a platform well suited to the integration of components for the most demanding systems and empowers system integration and design to ascend to higher layers of the Open Systems Interconnection (OSI) protocol stack, thus reducing system integration time.

Objectives of the CompactPCI Packet Switching Backplane

The objective of the CompactPCI/PSB Specification is to define an IEEE 802.3-2000 1000BASE-T compliant packet switching backplane to supplement the existing suite of PICMG 2.x Specifications. This provides designers, manufacturers, and integrators with a common platform for implementing an ESAN that provides all the benefits of a Local Area Network (LAN) in an embedded system environment. An ESAN can provide high-availability by providing redundancy in both interconnections and switching components.

Use of IEEE 802.3-2000 provides an industry-standard framework for network communication within the chassis that inherently follows the rules set forth in the OSI Reference Model (see Figure 1). OSI divides network communications processes into seven components called layers. Every layer consists of protocols for communicating with the preceding and succeeding layers. The CompactPCI/PSB Specification leverages IEEE 802.3-2000 1000BASE-T in providing the physical and data link layers. Protocol stacks such as TCP/IP can be added at the network and transport layers to provide a reliable connection-oriented environment.

![Figure 1 OSI Reference Model](image)

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CompactPCI/PSB is bit-rate scalable; a single pinout supports a physical interface at rates of 10, 100, or 1000 Mbps on a slot-by-slot basis (up to two links per slot). The CompactPCI/PSB supports full-duplex bit rates of up to 2000 Mbps per slot. A twenty-one slot PSB supports a total bandwidth approaching 40 Gbps. Redundant switching fabrics allow for the creation of High Availability (HA) systems. Connector and connector pin utilization is minimized (16 active pins on P3/J3), thus allowing all PICMG 2.x Specifications to coexist on P1/J1, P2/J2, P4/J4, and P5/J5, with the exception of PICMG 2.3, because it has not been developed to support differential pair signaling.

The CompactPCI/PSB includes well-defined subsets so that economical low-end systems can be built. A twenty-one slot backplane can be scaled from 10 to 1000 Mbps per port, one to two ports per slot; two to nineteen (Node) slots per chassis; and one to two purpose-built (Fabric) slots.

PACKET SWITCHING BACKPLANE OVERVIEW

A Packet Switching Backplane is composed of Node Slots, Fabric Slots, and the Links that interconnect them. The PSB topology is a star (not a bus) as shown in Figure 2. Each line interconnecting a Node Board and Fabric Board represents a Link that is a 10/100/1000 Mbps full-duplex Ethernet connection. Node Boards communicate by transferring/receiving packets to/from the Fabric Board, which transfers the packet to/from one or more Node Boards. Thus, every Node Board can communicate with every other Node Board and form a fabric.

Figure 2 Single Fabric PSB Topology

Figure 3 shows the physical interconnections after adding a second switch to the system and a second Link Port to each Node. Two Link Ports of a single Node Board are wired to each of the two Fabric Boards. An optional Link is defined between Fabric ‘a’ and Fabric ‘b’ that is 10/100/1000 Mbps capable.
Figure 3 Dual Fabric PSB Topology

Figure 4 shows a 19” chassis example. Chassis may support more or less than 21 slots. Fabric Slots may be located in any slot of the Packet Switching Backplane.

Node Slot Overview

Node Slot(s):

- Contain PSB Node Boards connected to one Fabric (‘a’) or both PSB Fabrics (‘a’ and ‘b’).
- Connections between Node Slots and Fabric Slots are via Links.
- Up to 19 Node Slots may be supported in a 19” CompactPCI/PSB backplane.
- A Node Slot may support 1 Link Port (‘a’) or 2 Link Ports (‘a’ and ‘b’), each @10/100/1000Mbps.
- Connection from each Node Slot to the CompactPCI/PSB Fabric Slot (‘a’ and ‘b’) is done via 16 active J3/P3 pins.
- Available bandwidth for each Node Slot can be up to 4 Gbps.

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**Fabric Slot Overview**

Fabric Slot(s) (‘a’ and ‘b’):
- Contain PSB **Standard Fabric Boards** connected with 1 to 19 PSB **Links**.
- Contain PSB **Extended Fabric Boards** connected with 20 to 24 PSB **Links**.
- **Fabric Boards** in **Fabric Slots** switch packets between multiple **Node Slots**.
- Connections between **Fabric Slots** and **Node Slots** are via **Links**.
- A **Standard Fabric Slot** may support between 1 and 19 **Links**, each @10/100/1000 Mbps.
- An **Extended Fabric Slot** may support between 20 and 24 **Links**, each @10/100/1000 Mbps.
- Up to 2 **Fabric Slots** may be supported in a CompactPCI/Packet Switching Backplane.
- Connection to the **Standard Fabric Slot(s)** is done via 152 active J3/P3, and J5/P5 pins.
- Connection to the **Extended Fabric Slot(s)** is done via 192 active J3/P3, J4/P4, and J5/P5 pins.
- Available bandwidth for each **Standard Fabric Slot** can be up to 20 Gbps (40 Gbps full-duplex).
- Available bandwidth for each **Extended Fabric Slot** can be up to 25 Gbps (50 Gbps full-duplex).
- **Link Port ‘f’** supports an optional Fabric ‘a’ to Fabric ‘b’ connection.

**Link Port Overview**

Figure 5 shows how Link Ports are defined for Node and Fabric Slots/Boards.

![Figure 5 Link Ports for Node and Fabric Slots/Boards](image)

**Link Overview**

Figure 6 shows an example of a 6-slot Dual Fabric Packet Switching Backplane.
Link Port ‘a’ of each Node Slot is connected to a Link Port of Fabric Slot ‘a’. Link Port ‘b’ of each Node Slot is connected to a Link Port of Fabric Slot ‘b’. Link Ports of Node Slot N are connected to Link Port N of Fabric Slots ‘a’ and ‘b’.

Hot Swap Interoperability

The CompactPCI/PSB Specification supports Hot Swap in several ways. PICMG 2.16 Boards and Packet Switching Backplanes may support only CompactPCI/PSB Link Ports or both the CompactPCI Bus and the CompactPCI/PSB Link Ports.

A new signal, PCI_PRESENT#, is defined for use by CompactPCI/PSB Boards. This signal is allocated to the P1/J1 connector on pin B6. P1-B6 is defined as ground (GND) in PICMG 2.0 R3.0. PCI_PRESENT# serves two purposes. It allows a board’s CompactPCI Bus interface to be appropriately configured when the CompactPCI Bus is not connected to the corresponding slot. In a Hot Swap environment, it partially determines when the board must locally manage the handle switch, Blue LED, ENUM# and quiescence of critical board resources. When low, this active-low signal indicates that the CompactPCI Bus signals are connected to the corresponding slot.

The complete 2.16 specification defines CompactPCI/PSB Hot Swap requirements for Backplanes, Node Boards and Fabric Boards with Hot Swap capabilities. A CompactPCI/PSB Hot Swap Board can support only CompactPCI/PSB Link Ports or both the CompactPCI Bus and the CompactPCI/PSB Link Ports. A Packet Switching Backplane Slot can support only CompactPCI/PSB Links or both a CompactPCI Bus and the CompactPCI/PSB Links.

PICMG 2.16 supports a superset of the High Availability functionality defined by PICMG 2.1. Not every implementation of PICMG 2.16 CompactPCI Packet Switching Backplanes or CompactPCI/PSB Hot Swap Node/Fabric Boards is necessarily interoperable with PICMG 2.1 defined High Availability components.
Node Board J3 Pin Assignment

The following table is provided for reference only and must not be considered adequate for design purposes. A proper understanding of isolation requirements, pin usage requirements, etc is necessary in order to create a PICMG 2.16 compliant product.

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