Physics Design Guide
for
Clocks, Gates & Triggers
in
Instrumentation

PDG.0 R1.0
23 April 2013

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Suggestions

SUG 7-1 The clock board in Slot 3 should provide the clock interface on all Channels (1 to 13[15]).

SUG 7-2 A bidirectional switch (e.g. FET based, or just 0R selection strap resistors) should be included onboard to isolate clock signals from Channels 1 and 2 (dark grey cells on Table 7-2) for compatibility when using the board in implementations that use standard fabric data hubs in Slots 1 and 2.

SUG 7-3 If it is foreseen to ever use the connection from Slot 1(2) to the timing board in Slot 3 as a standard data interface, a bidirectional switch should be used to select between outbound clock signals or inbound data signals (e.g. to an onboard FPGA Ethernet port) on Channel 1(2).

SUG 7-4 On the node boards installed in Slot 5 to 14, a 2:1 switch should be added to select between Channels 3 or 4.

SUG 7-5 If channels to Slots 1 and 2 are to be selected alternatively for clock or for data, a 3:2 switch should be added on the node boards to select between Channels 2, 3 or 4 (for node boards installed in Slot 1 or 2 at least).

SUG 7-6 If signal glitches are to be avoided in the process of switching, then circuitry for synchronous switching of clocks should be added (e.g. as in Figure 7-2). The logical device used to perform this function (e.g. FPGA) will need to also implement specific circuitry for fail-free switching of MET, WET or TSS type signals (e.g. switching of packet/word).

SUG 8-1 Boards that implement clocks on either the Fabric Channel or Update Channel should include a Board Point-to-Point Connectivity Record with an OEM GUID per Channel or Port configuration supported and Link Descriptors with the Link Class field set to 111b (OEM GUID Definition) and the Link Type field set to the appropriate OEM GUID index value 0000b-1110b. The Link Type Extension (LEXT) should be set to 0. This will protect boards that use clocking on the Fabric or Update channels from boards that use these channels for other purposes.

SUG 8-2 When a board is powered up, clock drivers should be disabled and placed in a high impedance state. This will eliminate the possibility of two boards driving the same clock line.

SUG 8-3 Boards with clock inputs should be designed to eliminate chatter or spurious triggering in the event that another board in the system is not driving clock line.

SUG 8-4 Board suppliers should provide driver or API code to configure clocks.

SUG 8-5 The clock driver/API should allow configuring of clock signal direction to the extent that it is supported by hardware.

SUG 8-6 The clock driver/API should allow enabling/disabling clock drivers.

SUG 8-7 The clock driver/API should allow configuring of timing/frequency to the extent that it is supported by hardware.

SUG 8-8 Upon a Board reset, clocks should remain running.

SUG 8-9 Upon a Board reset, clocks should maintain their state from the last configuration.
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1 Introduction

1.1 Intended Audience

This design guide is intended for electronics and software engineers that are designing systems for physics research and machine control systems. The ideas may find uses in other areas and designers should feel free to use the ideas presented herein.

1.2 Reference documents

The publications cited in this section are relevant to this specification. Most of the specifications referred to are subject to periodic and independent updates, and are the responsibility of their respective organizations. The reader is advised to check carefully the version or revision of the referenced specification that is to be used in conjunction with this document.

1.2.1 PICMG reference specifications

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<tr>
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<td>PICMG</td>
<td><a href="http://www.picmg.org/">http://www.picmg.org/</a></td>
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<td><a href="http://www.picmg.org/">http://www.picmg.org/</a></td>
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1.2.2 Other documents

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<tr>
<td>IEEE 40GBASE-KR4</td>
<td>IEEE</td>
<td></td>
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</table>

1.3 No special word usage

Unlike a PICMG specification that assigns special meanings to certain words such as “shall”, “should” and “may”, there is no such usage in this document. This document does have suggestions to enhance compatibility between designs using the information in this document. These appear as “SUG #-#” in the text similar in manner to “REQ #-#” in PICMG specifications and use the word should (in bold).
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1.5 Signal naming conventions

All signals are active high unless denoted by a trailing # symbol. Differential signals are denoted by a trailing + (positive) or – (negative) symbol.

All slot numbers are logical, not physical.

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1.7 Special terms and Acronyms

The following terms and acronyms are used in specific ways throughout this document.

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
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<tbody>
<tr>
<td>PTP</td>
<td>Point to Point</td>
</tr>
<tr>
<td>MET</td>
<td>Message Encoded Timing</td>
</tr>
<tr>
<td>WET</td>
<td>Word Encoded Timing</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low-voltage differential signaling</td>
</tr>
<tr>
<td>M-LVDS</td>
<td>Multipoint LVDS</td>
</tr>
<tr>
<td>CML</td>
<td>Current Mode Logic</td>
</tr>
<tr>
<td>LVECL</td>
<td>ECL referenced to 0V</td>
</tr>
<tr>
<td>LVPECHEL</td>
<td>ECL referenced to Positive Voltage</td>
</tr>
<tr>
<td>CGT</td>
<td>Acronym for Clocks, Gates and Trigger</td>
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1.8 Revision history

<table>
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<tr>
<th>Date</th>
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<tr>
<td>23 April, 2013</td>
<td>R1.0</td>
<td>Initial Release</td>
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# 2 Physics Clocks, Gates, Triggers and Timing

1. Physics needs clocks, gates, triggers and time-stamp signals for many control and data acquisition systems. For the purpose of this document all will be referred to as clocks unless clarity demands the specific name.

2. Clocks are as usually thought of as repetitive wave-forms at a constant frequency. Gates are signals that are used to enable electronics to process information. Gates are typically used to immunize the electronic system to external signals from periods of time when nothing of interest is happening or external “noise” should be ignored by the system. Triggers are signals that indicate that an event has occurred and some action should be taken such as recording some data. Time-stamps are sets of bits containing a time value that can be attached to the data. The time value can be transmitted through a single line such as Inter-Range Instrumentation Group (IRIG) time codes.

3. All of these signals can have stringent timing properties associated with them and therefore have been lumped together. Of the four, gates typically have the loosest timing requirements. Triggers and clocks have the highest accuracy requirements and in some uses have similar specifications.
3 PICMG 3.0 (ATCA) Bused Clocks

4 The information in this section is based on PICMG 3.0, Section 8 (Zone 2 Electrical Design Guidelines).

5 Three redundant differential bused clocks known as Synchronization Clocks are specified in PICMG 3.0. In one method the clock lines are routed on the backplane to every slot in sequence. PICMG 3.0 in Section 8.2.5.1 discusses a clock distribution scheme that skips every other slot, doubles back and picks up the skipped slots. This lengthens the line, changes the impedance and affects the delay. No delay effects are discussed so this discussion looks at the other effects.

6 Computing the line impedance, capacitance and other characteristics of traces can require special tools. For this discussion one can use some simple formulas that will show the various effects of line loading. The simple equation for the propagation delay on a loaded transmission line is:

\[
t_{pd} = t_{pd0} \sqrt{1 + \frac{C_d}{C_0}}
\]

Where \( t_{pd0} \) is the intrinsic propagation delay per unit length, \( C_0 \) is the intrinsic capacitance per unit length and \( C_d \) is the distributed capacitance per unit length. If the line is connected to every slot the delay is \( T_1 \). The delay for the skipped slots is \( T_2 \). With a bit of math we get the ratio as:

\[
\frac{T_2}{T_1} = \sqrt{2} \sqrt{\frac{2C_0 + C_d}{C_0 + C_d}}
\]

7 If \( C_d = 0 \) then \( T_2/T_1 = 2 \), the only effect is the line length. At the other extreme, if \( C_d >> C_0 \) then \( T_2/T_1 = 1.4 \) or 40% slower. If one assumes \( C_d = 4C_0 \) in the every slot loaded case and \( 2C_0 \) for the skipped slot case, then \( T_2/T_1 \) is \~1.5 or 50% slower. The main conclusion is that a line twice as long, loaded with the same number of boards, is not twice as slow.

8 The intrinsic (unloaded) impedance of a line is \( Z_0 \). The loaded line impedance \( (Z_L) \) is given by:

\[
Z_L = Z_0 \sqrt{1 + \frac{C_d}{C_0}}
\]

9 The impedance is not lowered as much in the skipped routing. For every slot vs the case of \( C_d = 4C_0 \) loading as above, the impedance is \~30\%
higher for the skipped slot routing. PICMG 3.0, Section 8.2.5.2 suggests that 130 Ω is better than 100 Ω since the impedance of the loaded line is higher and the line termination does not overload the drivers. The table below shows the results. The higher initial impedance results in a loaded impedance that is easier to drive and terminate.

**Table 3-1: Loaded Line Impedance**

<table>
<thead>
<tr>
<th>Routing</th>
<th>Z₀ ⇒</th>
<th>100 Ω</th>
<th>130 Ω</th>
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<tbody>
<tr>
<td>Every Slot</td>
<td>45 Ω</td>
<td>58 Ω</td>
<td></td>
</tr>
<tr>
<td>Skipped Slot</td>
<td>58 Ω</td>
<td>75 Ω</td>
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¶ 10 The system designer has to make some trade-offs when distributing clocks on bused lines as is shown in the discussion above. In any case, the driver should be in the middle of the line to minimize the delay to the end board. If a redundant board is used in the clock distribution then it should be in the next slot. Although, being able to place the clock driver in any slot may seem to be a good idea, this can cause some serious timing delay changes and signal degradation due to reflections.

¶ 11 Another problem with bused clocks is the variations in signals when boards are removed or added. The impedance goes up and down causing different distortions that go through the receiver threshold at different places in the signal. This results in timing shifts that can easily be several nanoseconds. The other effect is that the propagation delay from the driver to receiver will vary. Where precise timing of a few nanoseconds or less is specified, one will have to re-time the system.

¶ 12 The PICMG 3.0 document suggests that the maximum frequency is about 100 MHz for the clock lines. This is in general agreement with other data obtained from Fastbus and VME bused backplanes.

¶ 13 National Semiconductor Application Note 1503 specifically addresses the PICMG 3.0 M-LVDS clock buses and their applicable integrated circuits. These parts slower edges that compensates for capacitive effects but there is still the inherent bus loading problem discussed above.
4 PICMG 3.0 (ATCA) Radial Clock Distribution

¶ 14 Note that work by the PICMG Extensions committee may change or expand information in this section.

¶ 15 This section will discuss a much more precise and stable distribution system using radial lines. In some cases the bused clock may suffice for the system. However, if more precise timing is required then a radial clock distribution system may be necessary. The radial, or point-to-point distribution has fewer problems associated with adding or changing boards that are attached to the clock distribution. The impedance and propagation delay are constant. All boards are isolated from each other and therefore interaction between them is minimized.

¶ 16 Section 6.2.3.1 of the PICMG 3.0 discusses the channel transmission requirements. If some of these lines could be used for clocks they would have the best electrical characteristics of any lines in the backplane. The line impedance and delay changing is avoided since each line only sees a driver at one end and a receiver at the other. PICMG 3.0, Figures 8-5 thru 8-7 show insertion losses for radial lines in a full mesh configuration. Other radial configurations are similar. From these simulations the distribution of 3 GHz (maybe higher) signals should be no problem.

¶ 17 PICMG 3.0 assigns four lanes in each direction (8 pairs) to each radial channel connection. The aggregate bandwidth is at least 10 Gb/s in each direction. Many data acquisition and control systems do not require this high data bandwidth from a board so the number of lanes used can be reduced. The unused data lanes could then be assigned to high-speed clock distribution.

¶ 18 Trace routing requirements are fairly stringent in PICMG 3.0. In a differential pair the lines are to be matched within 3.4 ps. All four lanes in a channel are matched to within 140 ps. It should be noted that it is not sufficient to just match the physical length; the backplane manufacturing tolerances also come into play.

¶ 19 Propagation delay in FR4 is about 175 ps/inch (6.89 ps/mm). The trace length can be assumed as Manhattan length to a first approximation. This would give about 30 mm for the shortest traces between adjacent slots (e.g. Physical Slot 3 to slot 1) and 210 ps propagation delay. For one of the longest typical interconnects, from physical slot 7 to slot 14, we get about 260 mm Manhattan length (7 slots x 30 mm + 2 connectors vertically = 50 mm). One manufacturer reports that the true length of this trace on one of their backplanes is 235 mm or 1620 ps. This results in a Δt worst case of 1410 ps at the farthest receiver. This may not be a problem since it should remain constant. These calculations assume that Logical Slots 1 and 2 are physically located in the center and the worst-case
receiver at either end. If the clocks were redundant, the switch between driver boards (assume at the center) would cause about a 210 ps shift in the skew unless the backplane had extra trace length to compensate.

PICMG 3.0 backplane specification also defines ten signal pairs (Update Channels) that connect between pairs of boards. These lines are skew matched to similar accuracy as in the radial lines above. This is another possible precise timing channel between board pairs and should be considered by system designers for clocks, gates and triggers.
5 PICMG 3.0 (ATCA) Backplane Interconnections

5.1 Backplane General Information

PICMG 3.0 specification lists several interconnection options, Star, Dual Star, Dual-Dual Star and Mesh. These interconnects can be used for both data and clocks. Note that in this section the word clock also includes triggers, gates and time-stamps. Each Channel in PICMG 3.0 consists of 8 differential pairs, typically four assigned to each direction. The previous section discussed the high frequency characteristics of the point-to-point backplane wiring. This section does not consider the inter board data passing and computational issues. In general, this communication should not be affected by the clock discussion.

5.2 Dual Star Backplanes

First consider the Dual Star topology shown in Figure 1. This is probably the most common fabric topology in PICMG 3.0 backplanes. The one restriction is that the node and clock boards in the Dual Star configuration are restricted to specific slots, e.g. Logical Slots one and two.

Figure 5-1: Dual Star

5.2.1 Case 1: No redundancy and low bandwidth

For the case of no redundancy and low bandwidth the dual star would degenerate to a single star topology. All of the channel lanes are not needed and the extra lines can be used for clocks. Also, timing information can be embedded on the data lines (e.g. IEEE-1588, White-Rabbit, proprietary) allowing for full data transfer.
5.2.2 Case 2: No redundancy and high bandwidth

If redundancy were not needed for the system, one of the nodes could handle the fabric and the other the clocks. One would have eight pairs for clocks to each board.

5.2.3 Case 3: Redundancy and low bandwidth

If redundancy was necessary but the data bandwidth did not require four lanes, some of the lanes could be assigned to clocks. One would have redundancy for both data and clocks. For example, one data lane in each direction would allow up to six lanes for clock usage to each board. In some Physics applications a 2.5 Gbd data path would suffice for front-end boards. However, other applications for ATCA on Physics target high performance systems with requirements for very high transfer rates. In some cases even x4 ports are not enough and higher bandwidth connections must be provided externally, e.g. x16 PCIe via the RTM.

5.3 Dual-Dual Star Backplanes

The next topology shown in Figure 5-2 is the Dual-Dual Star. In this case there are four hub/switch boards. This configuration can be used if there is a requirement for redundancy and the data bandwidth is such that lanes in the data channels are not available for clocks. Here two of the hubs are assigned to the fabric and the other two are for the redundant clock distribution. Each board would have up to eight redundant clocks. The backplane is slightly more complicated than the Dual Star.

The one restriction is that the node and clock boards in the Dual-Dual star configuration are restricted to specific slots, e.g. Logical Slots one thru four.

Figure 5-2: Dual-Dual Star
5.4 Mesh Backplanes

The most general topology is the full mesh shown in Figure 5-3. In this case all slots are radially connected to all other slots. If the full data bandwidth is not needed, the mesh topology allows node (and clock) boards to be placed anywhere. Again, the center of the backplane may be the best position to minimize delays. This convenience comes at backplane complexity and some cost increase. The clock sources could be included in a standard node board or on separate boards as previously discussed. Also the system could be configured for redundancy as required.

If the mesh topology required all the channel bandwidth, as might be the case in data processing, there would be no free lanes for clocks. This situation generally occurs later in the data acquisition process where the clocks, gates and triggers are no longer needed.

It should be noted that any of the Star configurations could be implemented on a mesh backplane.

5.5 Clock Driver and Fanout Circuits

Circuits used for clock drivers, triggers and gates need to be evaluated on their jitter from random data pattern testing when used for critical timing. Table 5-1 below lists some important parameters from clock driver/receiver manufacturers. This abbreviated table is for point-to-point clock distribution. Check the manufacturer’s data sheet for detailed design information.
### Table 5-1: Sampling of Clock Chips

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Max. frequency</th>
<th>Channel skew match</th>
<th>Prop delay</th>
<th>Output Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>National</td>
<td>DS90LV110AT</td>
<td>200 MHz</td>
<td>35 ps typ</td>
<td>2.8 ns</td>
<td>LVDS</td>
</tr>
<tr>
<td>National</td>
<td>LMK01000</td>
<td>1600 MHz</td>
<td>±4 ps typ</td>
<td></td>
<td>LVDS</td>
</tr>
<tr>
<td>IDC</td>
<td>PCIe types</td>
<td>500 MHz</td>
<td>50 ps typ</td>
<td>4.5 ns</td>
<td>LVDS</td>
</tr>
<tr>
<td>Texas Inst</td>
<td>CDCLVP111</td>
<td>3500 MHz</td>
<td>15 ps typ</td>
<td>300 ps</td>
<td>LVPECL</td>
</tr>
<tr>
<td>ON Semiconductor</td>
<td>various</td>
<td>Up to 14 GHz</td>
<td>15 ps max</td>
<td>165 ps</td>
<td>CML</td>
</tr>
</tbody>
</table>

A number of clock driver integrated circuits listed above are geared to PCIe and high speed Ethernet. Many could be of more general use for Physics clocks, gates, and triggers.

### 5.6 PICMG 3.0 Transmission Line Simulations

A simulation report that was completed 18 November 2002 by PICMG on backplanes. Simulations that were done for radial and bused lines with various clock speeds and loadings. The information contained in the following link is for PICMG members only at this time. The link for the report is below. Non-members wishing to obtain a copy of the report should contact PICMG.

6 PICMG 3.0 (ATCA) Backplane Signals

6.1 Introduction

Accurate clock signals are required on the digitalization/reconstruction and control processes on Instrumentation devices. The PICMG 3.0 specification defines a small set of clock signals, which may be insufficient for many applications. Thus, a complementary clock interface specification may be required. The resources available on PICMG 3.0 for enhanced clock support, a performance comparison and required changes to the base Specification follow in the next sections of this document. The clock interface configuration disparities to PICMG 3.x shall be resolved by adding, when feasible, new Link Type/Extensions to the System Manager, to: (i) allow a compliant board to connect to any new clock interface and (ii) ensure compatibility with existing PICMG 3.x boards (see Chapter 8 for implementation). Table 6-1 shows the potential clock interface resources.

Table 6-1: Potential clock interfaces

<table>
<thead>
<tr>
<th>Clock Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronization Clock Interface</td>
</tr>
<tr>
<td>Shared Fabric Interface</td>
</tr>
<tr>
<td>Fabric Interface (Clock Hub)</td>
</tr>
<tr>
<td>Zone 3 Backplane Clock Interface</td>
</tr>
<tr>
<td>Update Channel Interface</td>
</tr>
<tr>
<td>Base Interface (encoded time)</td>
</tr>
<tr>
<td>Fabric Interface (encoded time)</td>
</tr>
</tbody>
</table>

6.2 Synchronization Clock Interface

Timing and synchronization support on PICMG 3.0 comprises only three bused clock ports: CLK1, CLK2 and CLK3 (see Figure 6-1). Each of these ports is composed of two identical functionality differential pairs, e.g. CLK1A and CLK1B, for timing redundancy applications. The ATCA boards access this clock bus through tri-state M-LVDS buffers and any board can be set as a Master clock generator. CLK1 and CLK2 are specified with fixed telecommunications frequencies (8 kHz and 19.44 MHz respectively) while CLK3 is user defined. Some fabric
protocols require clock synchronization (e.g. PCI Express with spread spectrum clocking) and CLK3 is often the choice.

![Clock Interface Diagram]

**Figure 6-1: Bused Clock Interface use example**

While the CLK1 and CLK2 use could be redefined, a total of only six bused differential pairs would be available for synchronization and limited to a maximum frequency of 100 MHz. The low speed Telco clocks (CLK1 and CLK2) are generally not of interest in Physics applications. Where Telco compatibility is not needed these could be assigned other frequencies and be more useful.

The interface does not use fabric ports thus full bandwidth can be preserved on fabric. However, it does not provide high quality, high-frequency point-to-point clock lines and slot to slot skew and delay will be dependant on the number and type of boards inserted.

### 6.3 Shared Fabric Interface

PICMG 3.0 fabric data channels provide up to four communication links (ports), each composed of two high performance differential pairs. Some of these point-to-point links may be reserved for carrying high performance synchronization signals; however, the channel data transfer rate capability would be proportionally reduced, which may be undesirable in some applications. New Link Types and Link Type Extensions will be defined for the Board's FRU Data that describe a new clock Link Type. The combination of the Link Type, Link Type Extension, and Link Designator will allow the use of up to 4 data Ports and up to 4 clock Ports in a single Channel. Note that the number of data ports plus and the number of clock ports cannot exceed 4. It will also be possible to add a
Link Class to new Link Types and Link Type Extensions that would restrict their use to backplanes that support 10.3125 Gbd (5.15625 GHz) signals (see Chapter 8).

This interface is compatible will all fabric configurations including dual-star. All nodes can receive/send up to 6 or 3 redundant high-quality point-to-point clock signals.

6.4 Fabric Interface (Clock Hub)

A PICMG 3.0 fabric channel can be used exclusively for interfacing the synchronization signals. With this approach up to eight, high performance point-to-point differential pairs (maximum frequency higher than 3 GHz and foreseeable jitter lower than 100 ps) are available on each board to carry synchronization signals to/from a central timing hub.

When no specific Hub Board is required on Slot 1(2), a Clock Hub Board can be inserted in Slot 1(2) to provide a (dual-)star of point-to-point clock ports to the 13[15] Node Boards (12[14] in redundant systems). This hub is non-standard (unlike Ethernet or PCIe hubs) but the approach is functional if all other Node Boards accept the clock interface in Port 1(2).

A Clock Hub Board should be inserted in Slot 3, (redundant on slot 4). The Clock Hub Board uses fabric Channels 3-15 as point to point bidirectional links to the node Boards on Slots 4-16, which interface the clock ports in Channel 3, (or redundant Channel 4). The Clock Hub Board generates clock signals locally and distributes them to the Node Boards and/or route any clock signal from any node board to any other Node Board(s) (broadcast, multicast or point-to-point). This clock interface is compatible with both dual-dual star and full-mesh backplanes but cannot be used on dual-star fabric backplane. This configuration is for implementations where one requires full data bandwidth from the Node Boards to the data hub in Slot 1(2) and the Clock Board in Slot 3(4) requires data connections (e.g. to setup the Boards). In this configuration, nodes should be able to receive clocks on channels 3 and 4.

6.5 Zone 3 Backplane Clock Interface

A Zone 3 backplane can be designed to provide an alternate, independent path for clock signals. These signals can be connected from the main ATCA Front Board using J33 (e.g. as a clock interface plug on ARTM) – while keeping RP30 and RP31 connected to the RTM. J32 (if present) may remain on the Front Board. 40 differential pairs would then be available, allowing one to implement, for example, a full-mesh of clock signals, with 2 differential pair ports connecting any pair of boards.
(2*13= 26 lines), plus 14 bused clock lines on J33 and another 40 pairs for the user on J31 of the Front Board connecting to RP31 on the RTM.

¶ 44 The backplane can be designed for low crosstalk noise and equal length lines allow excellent jitter and skew performances.

¶ 45 This clock interface main advantage is the provision of an independent signal path that does not limit the data interface performance for any fabric configuration; however it has some drawbacks:

- requires specifying and designing a backplane for clocks, perhaps voiding the use of the Zone 3 Backplane area for other applications;
- will increase system cost;
- will reduce the number of lines available on the RTM (just J31 is available) for the other functions.

¶ 46 The preferable option is to provide for a Zone 3 Backplane with only P33 connectors present. Due to the extremely tight tolerance requirements (considered not manufacturable) the RP32 connector needs to be removed. This will allow that the RP31, the Power Connector RP30 and the alignment/keying pin can directly connect with the Front Board.

¶ 47 The placement of the air flow seals in PICMG 3.8, Figure 2-6 will need to have their position adjusted to compensate for the clearance notch and the missing RP32.

¶ 48 Figure 6-2 shows a Zone 3 backplane with P33. This drawing is to be used as an aid to the backplane designer. The critical dimension is important for proper mating of the Zone 2 connectors and P33. Figure 6-3 shows the modified RTM edge to clear the Zone 3 backplane. PICMG 3.8, Figure 2-5 should be consulted for other required RTM dimensions. Details of the mounting the Zone 3 Backplane can be found in PICMG 3.0, Section 2.6.2.
Figure 6-2: Zone 3 Backplane with P33 ADF Connector
The user is free to design a backplane that covers the entire Zone 3 area. This full Zone 3 Backplane may have connectors that do not mate with an RTM (which is therefore unnecessary). Another option is to have the connector pins extend from the Front Board side of the Zone 3 Backplane through the backplane and mate with connectors on an RTM. This requires a new RTM design that has different dimensions and is sensitive to the thickness (and tolerances) of the backplane. The RTM and matching connector has to take into account these tolerances and insure a safe wipe. This document makes no attempt to specify such a system.

6.6 Update Channel Interface

The update channel interface, comprising ten differential connections, is not used in many applications. PICMG 3.0 could be amended to redefine these connections to carry synchronization signals. This redefinition
implies the design of new compliant backplanes eventually incompatible with current boards. However, it provides an opportunity for specifying new equal-length and low cross-talk lines for high performance synchronization signals transmission (this approach can nonetheless be used for the previous option).

6.7 Base Interface (encoded time)

¶ 51 Node Boards may implement an IEEE-1588 over Ethernet endpoint, thereby synchronizing a local disciplined clock and an absolute time counter to an IEEE-1588 grandfather clock through the 10/100/1000BASE-T connections on the Base Interface.

¶ 52 The interface does not use fabric ports thus fabric full data bandwidth can be achieved. Also, it is compatible to dual-star backplanes and provides support for redundancy as it uses standard Ethernet hubs. However it provides only a time synchronization mechanism, which may have higher jitter than required.

¶ 53 The interface can be used as complementary or substitute of other clock interfaces if the time accuracy attained is adequate for the application. Fractional frequency clock signals can be originated from the local disciplined oscillator through the use of a programmable PLL. Trigger and Gate signals can be generated by arithmetic comparison of the local synchronized time counter to pre-programmed time values. Asynchronous triggers are not supported.

6.8 Fabric Interface (encoded time)

¶ 54 An alternative to the Shared Fabric Interface is the use of in-band data protocols able to carry timing information, which usually require only a small fraction of the fabric channel bandwidth. The PICMG 3.1 Ethernet specification (XAUI, IEEE 10GBASE-KX4, IEEE 10GBASE-KR and 40GBASE-KR4), PCI Express or Serial RapidIO connections on the Fabric Interface can be used to transport time-coded messages. IEEE 1588 or White-Rabbit are the choices for the Ethernet protocol. Currently no PCIe or SRIO standard time coding implementations are known, but PTP-like encoded time protocols implementations are feasible.

¶ 55 This interface is compatible to dual-star backplanes and provides support for redundancy as it uses standard hubs. However, it just provides a time synchronization mechanism, which may have higher jitter than required. Implementations of these protocols over 10GBASE-KR or 40GBASE-KR4 (10.3125 Gbd per lane, 64B/66B signalling) will allow better accuracies. See PICMG 3.1 for requirements to use the 10.3125 Gbd signalling.

¶ 56 The interface can be used as complementary or even as a substitute of other clock interfaces if the time accuracy attained is adequate for the
Fractional frequency clock signals can be originated from the local disciplined oscillator through the use of a programmable PLL. Trigger and Gate signals can be generated by arithmetic comparison of the local synchronized time counter to pre-programmed time values. Asynchronous triggers are not supported.

### Table 6-2: Summary Of The Clock Interfaces

<table>
<thead>
<tr>
<th>Timing interface</th>
<th>Ports</th>
<th>Lines available</th>
<th>Performance</th>
<th>Compatibility</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Synchronization Clock Interface</strong></td>
<td>CLK1, CLK2 re-assigned. CLK3 user definable.</td>
<td>6 bused diff pairs</td>
<td>Fair 100 MHz</td>
<td>Compatible</td>
</tr>
<tr>
<td><strong>Shared Fabric Interface</strong></td>
<td>Clock and Data lines share a fabric port.</td>
<td>All nodes receive/send up to 6 distinct clock signals</td>
<td>Good ~3 GHz radial &lt;100 ps jitter</td>
<td>Changes to PICMG 3.0 required. Lowers the data rate.</td>
</tr>
<tr>
<td><strong>Fabric Interface (Clock Hub)</strong></td>
<td>Timing hub in slot 3;4 Ports 3;4 on Node Boards</td>
<td>All nodes receive/send up to 8 distinct clock signals</td>
<td>Good ~3 GHz radial &lt;100 ps jitter</td>
<td>New e-Keying type may be required.</td>
</tr>
<tr>
<td><strong>RTM Zone 3 Backplane Clock Interface</strong></td>
<td>Full-mesh of clock ports on J33 of Zone 3 (RTM).</td>
<td>Full-mesh of two P2P lines; 14 bused lines.</td>
<td>Excellent^2 Low skew Low jitter</td>
<td>Compatible.</td>
</tr>
<tr>
<td><strong>Update Channel Interface</strong></td>
<td>Update channel ports redefined for timing.</td>
<td>Up to 10 additional, equal length, low crosstalk diff pairs.</td>
<td>Excellent^2 Low skew Low jitter</td>
<td>Not compatible if update channels are used. Requires new backplane.</td>
</tr>
<tr>
<td><strong>Base interface (encoded time)</strong></td>
<td>Ethernet hub in Slot 1 (and 2).</td>
<td>IEEE-1588 time encoded on Ethernet. Disciplined clock and time signals.</td>
<td>&lt;50 ns rms time stamp jitter Very low clock jitter</td>
<td>Compatible.</td>
</tr>
<tr>
<td><strong>Fabric Interface (encoded time)</strong></td>
<td>Ethernet/PCIe/ SRIO hub in slots 1 (and 2).</td>
<td>Time encoded on Ethernet/ PCIe/ SRIO. Disciplined clock and time signals.</td>
<td>Good^1 ~3 GHz, P2P &lt;100 ps jitter</td>
<td>Compatible PCIe/ SRO protocol unknown.</td>
</tr>
</tbody>
</table>

Note 1: Can be further improved with the implementation of equal length, low crosstalk lines on new backplanes.

Note 2: When equal length lines are used on backplanes and zero delay buffers on endpoint/hub boards.
7 Fabric Interface (Clock Hub in Slot 3)

¶ 57 This section focuses on the aforementioned clock distribution using the fabric interface with a Clock Hub Board in slot 3 or 4.

7.1 Overview

¶ 58 The clock distribution is centered on a star on PICMG 3.0 Slot 3 or a dual star centered on Slots 3 and 4 for redundant systems (see Figure 7-1). Dual-dual star or full-mesh backplanes may be used.

¶ 59 A Clock Hub Board, located in Slot 3 (optionally also in Slot 4), will be responsible for providing a point-to-point and bidirectional interface to each Node Board on the other slots (except Slot 1 and 2 that are reserved for data interfaces) and implement the following functions:

- Locally generate and distribute timing signals to the Node Boards or front panel.
- Routing any individual timing signal from/to the front panel and from any Node Board to any of the other Node Boards.
- Provide support for broadcast, multicast or point-to-point transmission of any inbound signal.

¶ 60 The 4x Fabric Channel can be partitioned in one 1x full-duplex communications Port for complex timing applications and three Ports (six differential pairs) for standard signals. Other configurations are possible,
some may be user defined. The suggested types of timing signals to be supported are shown on Table 7-1.

**Table 7-1: Timing Signals Types**

<table>
<thead>
<tr>
<th>Signal type</th>
<th>Signal description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Binary State Timing (BST)</td>
<td>Standard clock, trigger and gate type signals.</td>
</tr>
<tr>
<td>Word Encoded Timing (WET)</td>
<td>Synchronous time-multiplexed BST signals transported serially on an n-bit word, e.g. using 8b/10b word coding up to 8 signals can be multiplexed at 1/10 of the signalling rate. Signals synchronicity is kept but at a smaller bandwidth.</td>
</tr>
<tr>
<td>Message Encoded Timing (MET)</td>
<td>Deterministic timing messages (sequence of words) modulated as 8b/10b or 64b/66b signals. These messages may carry trigger/event signals transport, clock skew correction, and time adjustment messages. Signals synchronicity may not be kept.</td>
</tr>
<tr>
<td>Time Stamped Signal (TSS)</td>
<td>Serial one-line time information such as IRIG-B.</td>
</tr>
</tbody>
</table>

On the Clock Hub Hoard each of the three downstream differential pairs can be setup to carry clock, trigger/pulse, gate or time-stamp signals. The three upstream differential pairs can be used to send timing signals from each Node Board to the Clock Hub Board that routes them to a set of the other Node Boards. Other upstream/downstream partitions are possible. The Clock Hub Board behaves as a switch of timing signals, which has multicast/broadcast capability. Table 7-2 shows the Clock Hub connections to the Node Boards.
Table 7-2: Clock Hub Connections

<table>
<thead>
<tr>
<th>Logical Slot #</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
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<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
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<tr>
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<td>2-13</td>
<td>2-14</td>
</tr>
<tr>
<td>P22</td>
<td>1</td>
<td>2-1</td>
<td>1-2</td>
<td>1-3</td>
<td>1-4</td>
<td>1-5</td>
<td>1-6</td>
<td>1-7</td>
<td>1-8</td>
<td>1-9</td>
<td>1-10</td>
<td>1-11</td>
<td>1-12</td>
<td>1-13</td>
<td>1-14</td>
<td>1-15</td>
</tr>
</tbody>
</table>

Each cell within the table represents a Fabric Channel and the numbers within the cell represent the destination end-point to which that Channel is routed. For example, the cell representing Channel 1 of Slot 3 contains the value (1-2) to indicate it is connected to Channel 2 of Slot 1.

With this scheme any board can receive and/or generate up to three high-speed high-quality timing signals with a maximum frequency of half the rated baud rate of the backplane. For backplanes compliant with the PICMG 3.0 and PICMG 3.1 these specifications limit the upper frequency to 1.5625 GHz (half of 3.125 Gbd). For backplanes compliant with the PICMG 3.1, this specification limits the upper frequency limit to 5.15625 GHz (half of 10.3125 Gbd). Users should refer to PICMG 3.0 or PICMG 3.1 as appropriate for details on backplane and board properties. Skew compensation mechanisms may be used to lower skew figures. The recovered clock of the xET link clock and an almost limitless number of fast (sub-microsecond) trigger, events, or messages may be passed from/to any of the other boards.

Each Node Board will connect to the timing interface on the connector pairs of Table 7-3. As shown, each timing fabric channel provides up to three ports (BST1-BST3) and one xET port.

Table 7-3: Timing Interface Connector Pairs

<table>
<thead>
<tr>
<th>Interface</th>
<th>Connector Pairs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ab</td>
</tr>
</tbody>
</table>

Note 1: xET stands for either WET or MET (see Table 7-1)
Suggested differential signal electrical levels on the clock port are: LVDS, M-LVDS, CML, LVECL, or LVPECL.

MET signalling possibility could use PICMG 3.1 (Ethernet), PICMG 3.4 (PCI Express) or PICMG 3.5 (Serial RapidIO) Fabric Interfaces.

WET signalling possibility could use 8b/10b, 64b/66b or 128b/130b encoding.

TSS signalling possibility could use IRIG-B Direct Current Level Shift – DCLS (width coded) over LVDS.

Various Port Configuration options are possible as suggested in Table 7-4. For each port the signalling and levels can be those suggested \[64\] above.

<table>
<thead>
<tr>
<th>Option</th>
<th>Port 0</th>
<th>Port 1</th>
<th>Port 2</th>
<th>Port 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MET</td>
<td>CLOCK</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>WET</td>
<td>CLOCK</td>
<td>CLOCK</td>
<td>TSS</td>
</tr>
<tr>
<td>3</td>
<td>MET</td>
<td>CLOCK</td>
<td>TRIGGER</td>
<td>GATE</td>
</tr>
<tr>
<td>4</td>
<td>MET</td>
<td>CLOCK</td>
<td>TRIGGER</td>
<td>TSS</td>
</tr>
<tr>
<td>5</td>
<td>WET</td>
<td>CLOCK</td>
<td>TRIGGER</td>
<td>TSS</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

A Clock Hub Board can be designed for Slot 3(4) and keep clock channels to Slots 1 and 2, if:

SUG 7-1 The Clock Hub Board in Slot 3 should provide the clock interface on all Channels (1 to 13[15]).

SUG 7-2 A bidirectional switch (e.g. FET based, or just 0R selection strap resistors) should be included onboard to isolate clock signals from Channels 1 and 2 (dark grey cells on Table 7-2) for compatibility when using the board in implementations that use standard fabric data hubs in Slots 1 and 2.

SUG 7-3 If it is foreseen to ever use the connection from Slot 1(2) to the Clock Board in Slot 3 as a standard data interface, a bidirectional switch should be used to select between outbound clock signals or inbound data signals (e.g. to an onboard FPGA Ethernet port) on Channel 1(2).

The Node Boards connect to the clock interface (eventually through a bidirectional switch or selection straps) on:

- Channel 3, if the Node Board is inserted in Slot 4 to 14 (as per the 2nd number on the light grey cells of Table 7-2).
- Channel 2, if it is foreseen that the Node Board is inserted in Slot 1 or 2 (as per the 2nd number on the light grey cells of Table 7-2).
Table 7-5: Examples of chips to implement a 2:1 bidirectional switch

<table>
<thead>
<tr>
<th>Maxim IC</th>
<th>MAX4888A, MAX4889A, MAX4889B, MAX4889C</th>
</tr>
</thead>
<tbody>
<tr>
<td>NXP Semiconductors</td>
<td>CBTL04082A(B), CBTL04083A(B)</td>
</tr>
<tr>
<td>Texas Instruments</td>
<td>HD3SS3412, HD3SS3415, TS2PCIE412, TS2PCIE2212</td>
</tr>
</tbody>
</table>

¶ 71 As per the datasheets of the chips on Table 7-5, signals with a common mode voltage not higher than 2 V and less than 1.6 V peak-to-peak differential input voltages can be handled. This includes LVDS, CML and LVPECL. Pair-to-pair skew is typically lower than 60 ps.

7.2 Clock interface redundancy

¶ 72 On redundant systems, real-time selection of the clock channel may be required to switch from Slot 3 to Slot 4 Clock Boards when a fault occurs.

SUG 7-4 On the Node Boards installed in Slot 5 to 14, a 2:1 switch should be added to select between Channels 3 or 4.

SUG 7-5 If channels to Slots 1 and 2 are to be selected alternatively for clock or for data, a 3:2 switch should to be added on the Node Boards to select between Channels 2, 3 or 4 (for Node Boards installed in Slot 1 or 2 at least).

SUG 7-6 If signal glitches are to be avoided in the process of switching, then circuitry for synchronous switching of clocks should to be added (e.g. as in Figure 7-2). The logical device used to perform this function (e.g. FPGA) will need to also implement specific circuitry for fail-free switching of MET, WET or TSS type signals (e.g. switching of packet/word).
Figure 7-2: Glitch-free clock switching circuit example

7.3 Protocols for MET Type Signals

A number of protocols for the MET type signals can be used. Distinction parameters are: (i) time accuracy/signal jitter and (ii) channel to channel skew performance.

7.3.1 IEEE-1588 (PTP)

IEEE-1588 defines a point-to-point (PTP) protocol enabling precise synchronization of clocks in measurement and control systems. The synchronization algorithm relies on the exchange of time stamp messages from a Grandmaster unit containing the master clock to a PTP client containing the clock to be adjusted. The slave clock unit then calculates the average delay between the two clock units and adjusts the slave clock to the correct time value.

Current implementations of PTP over Ethernet provide time synchronization with accuracy as low as 50 ns RMS. PTP is independent of link delay, works with non-synchronous networks but does not provide fine delay adjustment.

7.3.2 Proprietary synchronous protocols

Proprietary protocols can be tailored for maximum timing performance and higher-level synchronization protocols (e.g. PTP) and link delay compensation can be straightforwardly added. Examples are:

7.3.2.1 DESY

DESY system wide synchronization (µTCA) for XFEL, which allows skew in the picosecond range. The system distributes a master clock with encoded data in a multiple star topology. A receiver can redistribute the signals including a link length compensation to achieve ps stability. The encoded data contains synchronization, trigger delays, free define-able
The synchronization signal is used to keep different clock dividers in a large system at predictable phases. Clocks can be shifted on receivers in sub-ps steps and trigger delays with ns resolution. Gates, clocks, triggers and data are available on the front panel, the backplane and on an optional MTCA.4 Rear Transition Board. See Section 9 for reference on uTCA or MTCA.4.

### 7.3.2.2 White Rabbit

White Rabbit uses hardware-assisted PTP for clock synchronization over Synchronous Ethernet (endpoints recover the COMM clock) and includes a line delay compensation mechanism. It synchronizes the slave clock with the master clock by measuring and compensating the coarse delay (using PTP) introduced by the link in multiples of 8 ns. All network nodes use the same physical layer clock (125 MHz, 8 ns period), generated by the Timing Master. Clock is encoded in the Ethernet carrier and recovered by the PLL in the physical network layer. Fine delay adjustment is performed using a digital ‘Dual Mixer Time Difference’ that outputs a measure of the phase between master and slave clocks (re-transmitted to the master from the slave unit), which will then drive an adjustable delay element on the master unit to compensate the slave clock phase.

Currently White-Rabbit jitter figures for the time-stamps are better than 100 ps RMS. A time skew accuracy of ±350 ps (STD = 80 ps) over a 5 km fiber-optic point-to-point link was achieved.

### 7.3.2.3 CERN

The LHC Timing and Control (TTC) distribution system reaches a precision of about 80 ps RMS. It relies on a serial stream at 40 MHz sent to all experiments. This serial stream merges clock and trigger data on the same link. For the upgrade a new protocol (GBT) has been defined merging slow control, acquisition and time distribution on links running at 4.8 Gbits/s.

### 7.2.3 PTP Timing over PCIe or Serial RapidIO

PTP may be implemented on networks supporting multicast messaging including but not limited to Ethernet. PCIe or SRIO lower message time jitter makes then good candidates to provide the PTP network layer. Being inherently synchronous, link delay compensation mechanisms can also be added. No current implementations are known to exist.
7.4 Signal Integrity

Ideally the use of low crosstalk signal lines and low-noise, high-bandwidth electronics will result in good, low jitter timing signals. When this ‘passive’ approach isn’t able of providing the required quality timing signals on the endpoints, other options must be considered:

- Clock signals may be de-jittered using a PLL/VCXO de-jitter circuitry on the Node Boards (See Figure 7-3 & 7-4).

![Figure 7-3: Clock de-jittering circuit example](image)

- Triggers, sequences of pulses and gate signals may be de-jittered by sampling those signals with a de-jittered higher-frequency clock (a deterministic signal delay of \( \frac{1}{2} \) the clock period will be added).

![Figure 7-4: CGT signals de-jittering circuit example](image)

Trimmed length lines and zero delay buffers may provide uncomplicated skew adjustment, however automatic compensation, using a clock loop phase adjustment schema, can be used to compensate the slot-dependent propagation delays of up to 6 ns from the central to the end slots (the specified max delay on the PICMG 3.0 backplane between the end slots is 1.41 ns). Figure 7-5 shows a diagram of a possible implementation of the de-jittering and skew compensation schema. The best performance is
achieved when the RX path delay is similar to the TX path delay. A μTCA implementation using a similar concept was developed at the Stockholm University, Sweden.

Figure 7-5: Skew Compensation And De-Jitter Circuit example

7.5 Fabric Interface (Clock Hub) examples

Figure 7-6 shows an example of the implementation of a Clock Hub (signal buffers are not represented).

Figure 7-6: Example Of Clock Hub

The design in Figure 7-6 is centered on a cross-point multicast switch, which will route any of three BST signals from any Node Boards to any (number of) Node Boards. A timing switch implemented on an FPGA can route xET signals. Local generated signals or external (front panel) signals can also be input to the switches.
Figure 7-7 shows an example of clock interfaces implementation on an AMC carrier.

The design is centered on a cross-point switch, which routes any BST signal on the clock interface and Channels 3 and 4 of the PICMG 3.0 Zone 2 connector, as well as any signal from the clock interface and ports 17 to 20 of the AMC connectors to any of these timing interfaces. xET signals may be decoded on an FPGA and input to the BST switch to be routed to any the above-referred interfaces. The IPM controller queries the switches and program the BST buffers accordingly, as inbound or outbound lines.

Figure 7-8 shows an example of an IEEE-1588 and IRIG clock interfaces implemented on an AMC carrier.
7.6 Timing on an AMC.0 Carrier Board

The AMC.0 Carrier Board (Carrier) timing/clocking interconnections are be defined as in Sections 6.4 and 6.5 of MTCA.4 specification with the following modifications:

1) "MCH" word instances substituted by "Carrier";
2) "backplane" word instances substituted by "Carrier embedded timing bus";
3) replace text in ¶ 121 to read: "TCLKC and TCLKD are implemented in a similar manner to TCLKA and TCLKB and may be defined as its redundant clock lines".

Figures 7-7 and 7-8 shows examples of clock interfaces implementations on an AMC.0 Carrier Board.
8 Management Suggestions

8.1 Overview

Electronic keying (E-Keying) as defined in the PICMG 3.0 specification, provides a mechanism to ensure that Boards installed in the ATCA system can be appropriately powered and will not damage each other due to interconnection of incompatible interfaces. The clocking definitions included in this specification fall outside the current scope of PICMG Hardware Platform Management, therefore, additional care must be taken to ensure that Boards are not damaged through the interconnection of incompatible signals on the Fabric or Update Channels.

The committee recognizes that a complete E-Keying definition is a long-term necessity for the implementation of a PICMG standard regarding clocks for physics applications. That work, including intricacies of clock configuration management is the subject for possible future PICMG work. Until such a specification exists, however, the suggestions contained within this design guide will allow implementers to proceed with products in order to support physics application needs and gain better understanding of the clocking Hardware Platform Management requirements unique to physics.

8.2 Suggestions for Board Management

SUG 8-1 Boards that implement clocks on either the Fabric Channel or Update Channel should include a Board Point-to-Point Connectivity Record with an OEM GUID per Channel or Port configuration supported and Link Descriptors with the Link Class field set to 111b (OEM GUID Definition) and the Link Type field set to the appropriate OEM GUID index value 0000b-111b. The Link Type Extension (LEXT) should be set to 0. This will protect boards that use clocking on the Fabric or Update channels from boards that use these channels for other purposes.

Selection of OEM GUID values to enable multi-vendor interoperability is beyond the scope of this design guide.

SUG 8-2 When a Board is powered up, clock drivers should be disabled and placed in a high impedance state. This will eliminate the possibility of two Boards driving the same clock line.

SUG 8-3 Boards with clock inputs should be designed to eliminate chatter or spurious triggering in the event that another Board in the system is not driving clock line.

Once Boards are powered up, clocks will need to be configured for the particular system requirements and drivers will need to be enabled. There are several means to accomplish this including:
- Static configuration – Boards have a fixed configuration that cannot be altered. Suppliers of Boards must meet system requirements by design.
- Firmware configuration - Boards are configurable via serial eeprom or BIOS settings so that the clock configuration matches the system requirements.
- Software configuration – The Board programs the clock configuration using driver settings or API calls.
- Management software – An external management agent (clock manager) programs the clocks.

Related to the configuration of clocks, this design guide makes the following suggestions:

SUG 8-4 Board suppliers should provide driver or API code to configure clocks.
SUG 8-5 The clock driver/API should allow configuring of clock signal direction to the extent that it is supported by hardware.
SUG 8-6 The clock driver/API should allow enabling/disabling clock drivers.
SUG 8-7 The clock driver/API should allow configuring of timing/frequency to the extent that it is supported by hardware.
SUG 8-8 Upon a Board reset, clocks should remain running.
SUG 8-9 Upon a Board reset, clocks should maintain their state from the last configuration.

Note that power cycling of a Board is equivalent to insertion and E-Keying conditions apply.
9 Clocks, Gates and Triggers with μTCA

MTCA.4 is a PICMG specification that defines a Rear Transmission Module and a μTCA shelf for use with double-wide AMCs. Several options are available to the user of MTCA.4 specification. See PICMG MTCA.4 (22 September 2011) with Errata of 1 August 2012.