CorEdge NETWORKS

5 Gbps "DOUBLE CAP" PCI-EXPRESS SIMULATION AND ANALYSIS

SUMMARY:

This report documents frequency domain simulation to quantify the effect of the additional capacitor and its launch on the module-carrier-module Gen 2 PCI Express implementation. Plots of the channel insertion loss (SDD21), return loss (SDD11) and impulse response are documented, specifically focusing on 2.5 GHz, the fundamental frequency for a 5 Gbps bandwidth.

The capacitor launches and associated via models were created in Ansoft HFSS version 10. The launches were optimized and via stubs minminzed to represent a realistic, well designed 5 Gbps implementation.

The optimized passive channel with 1.0μF, 0.68μF or no cap yielded nearly identical frequency domain performance.

Assumptions for the Simulations:

1. HSPICE compatible models of the AMC B+ connectors were supplied by Yamaichi in S-Parameter format.

2. The trace lengths and net configuration are shown in Figure 6 on Page 8. The data was provided by CorEdge.

3. FR4 material assumed a dielectric constant of 4.20 with a loss tangent of 0.021.

4. All circuit traces included frequency dependent losses and were modeled by converting the output from the Ansoft HFSS field solver to an H-SPICE compatible table model file format.

5. 0.1μF, 1.0μF and 0. 68μF caps, with a 0603 package and X7R dielectric material, were used to AC couple the links.

Stackups:

The 18 layer stackup used for the AMC module is shown in Figure 1 below. Internal trace width is 3.5 mils and external trace width is 4 mils.

Module Stackup

	Module Stackup		
1	Surf	0.0006/0.0012	
			0.0029
2	Plane	0.0006	
			0.0030
3	Plane	0.0006	
			0.0028
4	Signal	0.0005	
			0.0030
5	Signal	0.0005	
			0.0029
6	Plane	0.0005	
			0.0025
7	Signal	0.0005	
			0.0029
8	Signal	0.0005	
			0.0025
9	Plane	0.0005	
			0.0029
10	Plane	0.0005	
			0.0025
11	Signal	0.0005	
			0.0029
12	Signal	0.0005	
			0.0025
13	Plane	0.0005	
			0.0029
14	Signal	0.0005	
			0.0030
15	Signal	0.0005	
			0.0028
16	Plane	0.0006	
			0.0030
17	Plane	0.0006	
			0.0029
18	surf	0.0006/0.0012	
Differential Pair to be modeled as 3.5 mil trace			
Total Board Thickness			0.0630

Device via standard construction 8 mil diameter drill
All other vias standard construction 10 mil diameter drill

Figure 1: 18 layer stackup used for the AMC module.

The 20 layer stackup used for the carrier board is shown in Figure 2 below. Internal and external trace width is 4 mils.

Carrier Board Stackup

		Carrier Stackup			
	1	Surf	0.0006/0.0012		
				0.003	
	2	Plane	0.0006		
				0.003	
	3	Plane	0.0006		
				0.004	
	4	Signal	0.0006		
				0.004	
	5	Signal	0.0006		
				0.003	
	6	Plane	0.0006		
				0.0055	
	7	Signal	0.0006		
				0.0055	
	8	Plane	0.0006		
				0.0055	
	9	Signal	0.0006		
				0.0055	
	10	Plane	0.0006		
				0.0003	
	11	Plane	0.0006		
				0.0055	
	12	Signal	0.0006		
				0.0055	
	13	Plane	0.0006		
				0.0055	
	14	Signal	0.0006		
				0.0055	
	15	Plane	0.0006		
				0.004	
	16	Signal	0.0006		
				0.004	
	17	Signal	0.0006		
				0.004	
	18	Plane	0.0006		
				0.003	
	19	Plane	0.0006		
				0.003	
	20	Surf	0.0006/0.0012		
	Differential Pair to be modeled as 4.0 mil trace				
	Total Board Thickness			0.0950	

	All vias standard construction 10 mil diameter drill

Figure 2: 20 layer stackup used for the carrier.

Via Model Features:

Via pair models were created in Ansoft HFSS V.10 and are intended to be representative of a well designed implementation at 5 Gbps. As such, anti-pad geometry, via stub length and ground return vias were optimized.

The dimensions and feature sizes for the AMC module BGA vias are shown in Figure 3 below. A 1 mm BGA was assumed. For optimization:

- The via stub was minimized with connection on layer 1 and layer 15.

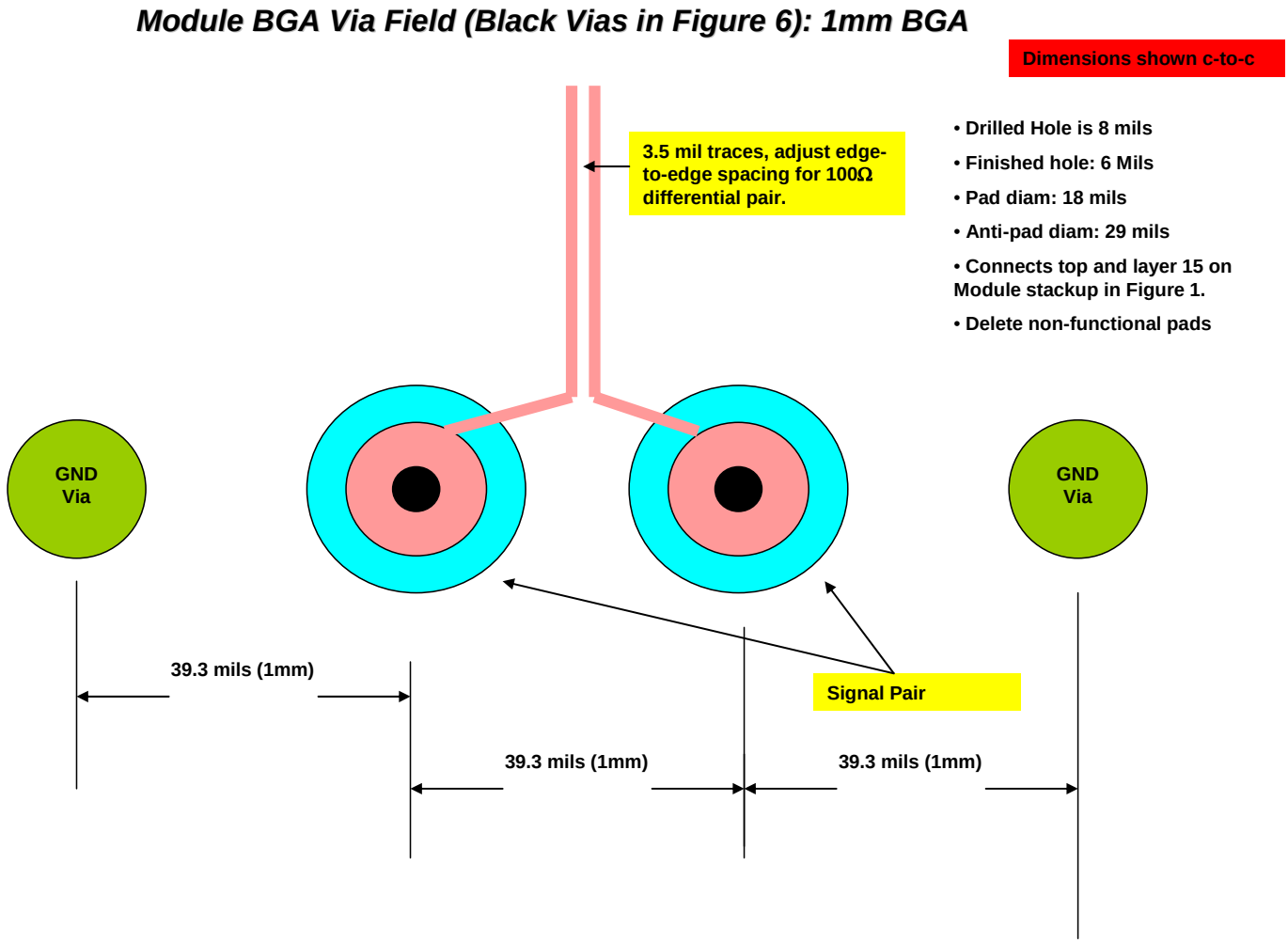

Figure 3: 1 mm BGA via dimensions.

The dimensions and feature sizes for the AMC module cap launch and associated vias are shown in Figure 4 below. For optimization:

- The 32 mil diameter anti-pad has been ovalized.
- Two ground return vias have been added 50 mils c-to-c from signal vias.
- Cap pads and cap body have been relieved on layer 2.
- Via stub minimized with connection on layer 1 and layer 15.

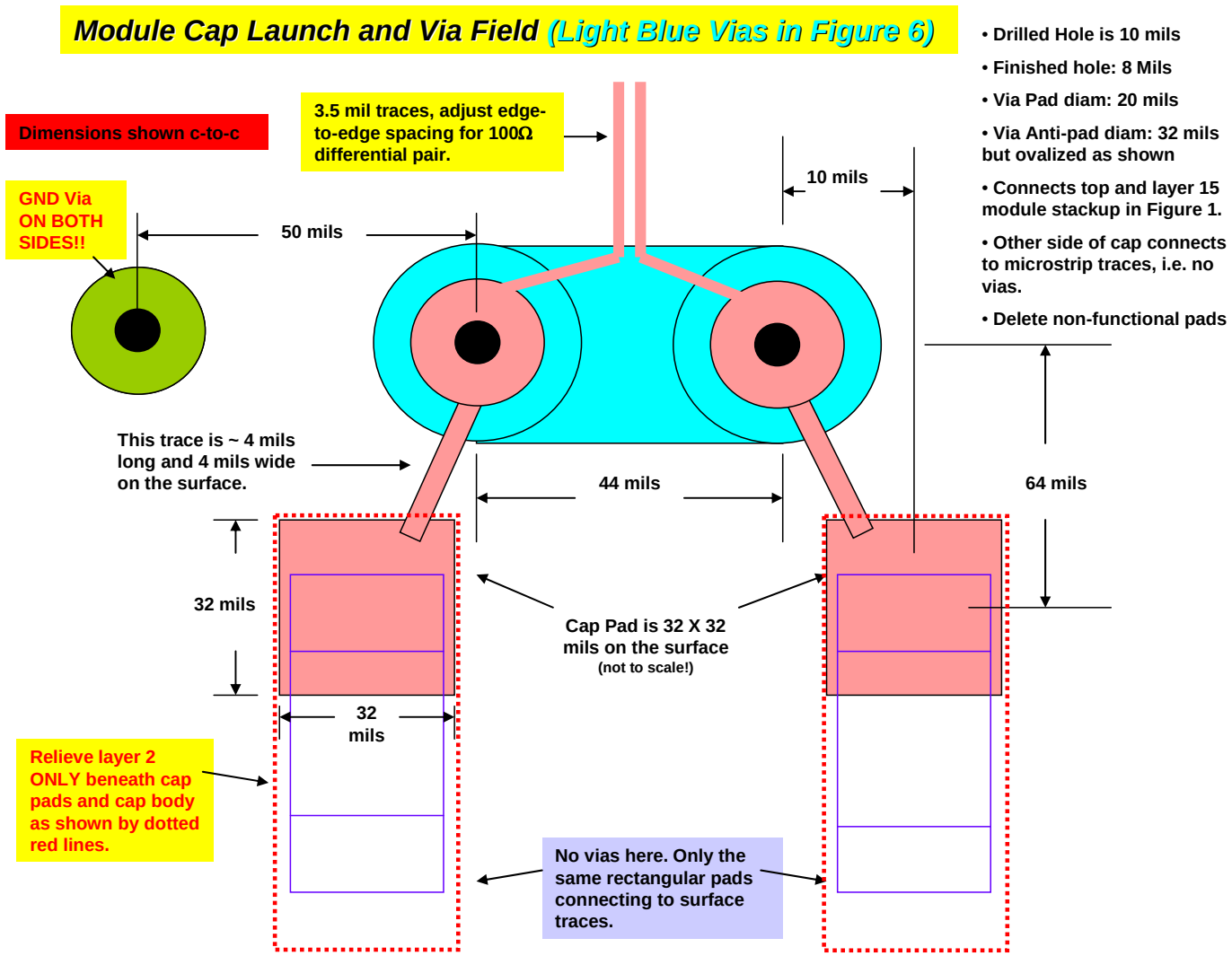

Figure 4: Module cap launch and via dimensions.

The dimensions and feature sizes for the carrier board AMC B+ connector vias are shown in Figure 5 below. For optimization:

- Via stub minimized with connection on layer 1 and layer 17.

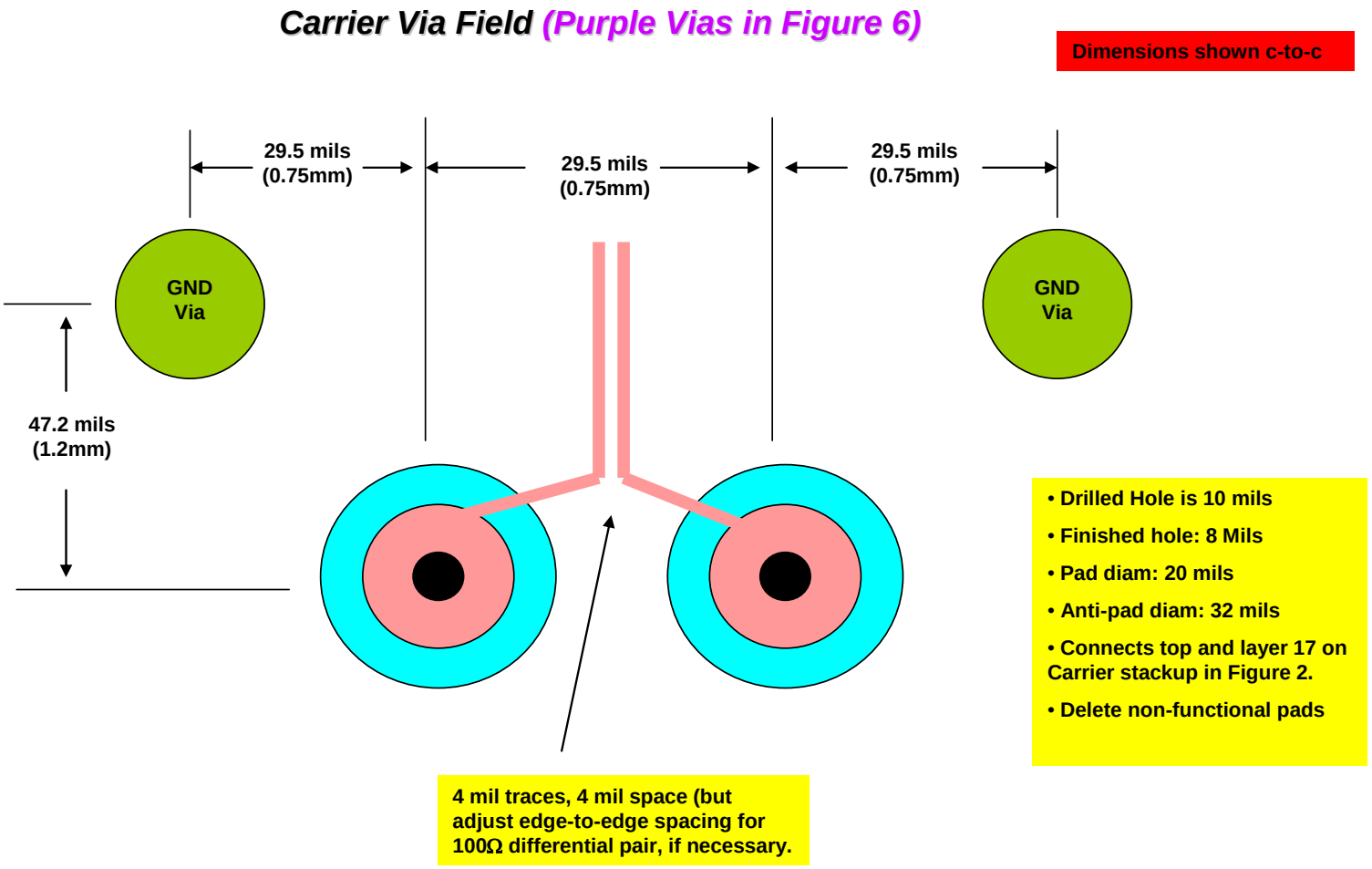

Figure 5: Carrier board AMC B+ connector via dimensions.

5 Gbps Module-Carrier-Module, Two Connector, AMC B+

The 5 Gbps module-carrier-module channel with two AMC B+ connectors is shown schematically in Figure 6 below. The longest link is a total of 16" long from buffer output to receiver input. Two different 0603 coupling cap values were simulated on the RX module board: 1.0µF and 0.68µF. The topology was also simulated with no capacitor on the receive side. For this case, the 0.3" microstrip traces were brought from the surface to internal layers with vias but there were no capacitor launch pads.

5 Gbps Gen 2 Module-Carrier-Module, Two Connector, AMC B+

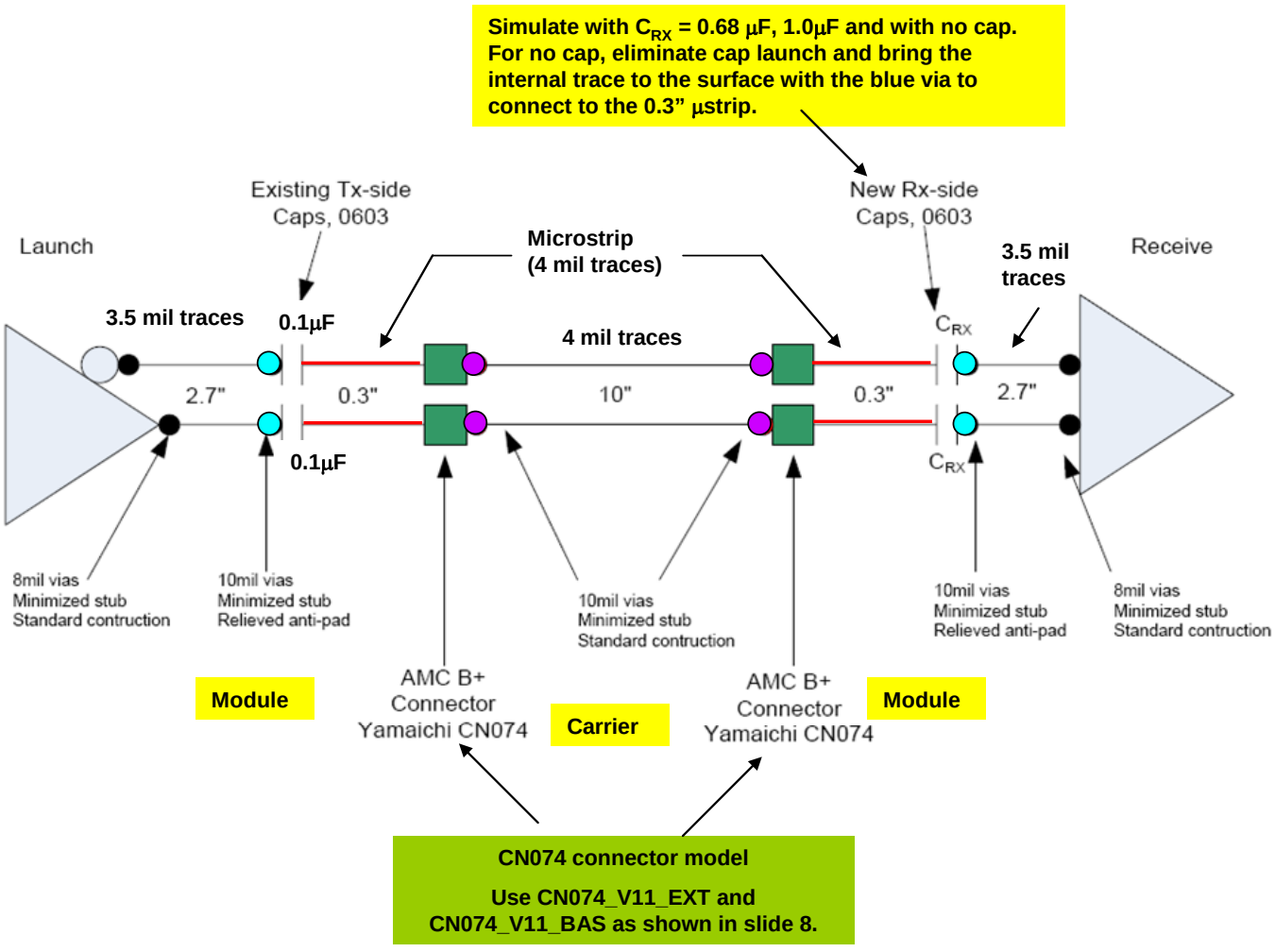

Figure 6: 5 Gbps Gen 2 Module-Carrier-Module Topology.

The insertion loss for the entire channel is shown in Figure 7 below. With the optimized vias and cap launch, it is virtually the same with and without the caps. Note that at the 2.5 GHz fundamental frequency the loss is about -11.0 dB. The insertion loss deviation is significantly less with the optimized vias and cap launch compared to the 2.5 Gbps link modeled which used a more worst-case implementation.

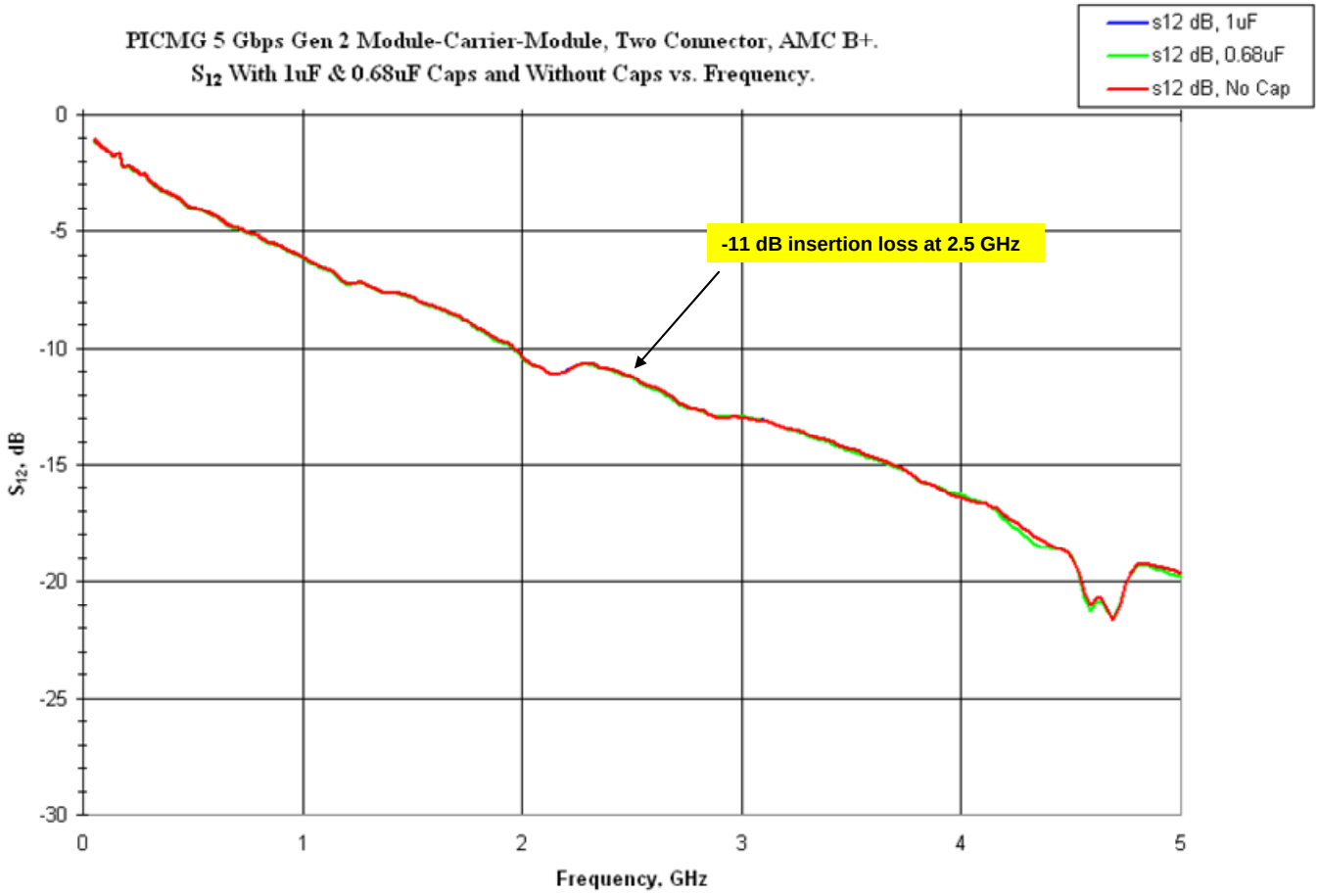

Figure 7: Insertion loss for module-carrier-module channel with and without caps.

Figure 8 below shows the return loss of the channel with and without the RX caps. The return loss is better than 12 dB for the entire frequency range. It is significantly improved over the original 2.5 Gbps channel implementation.

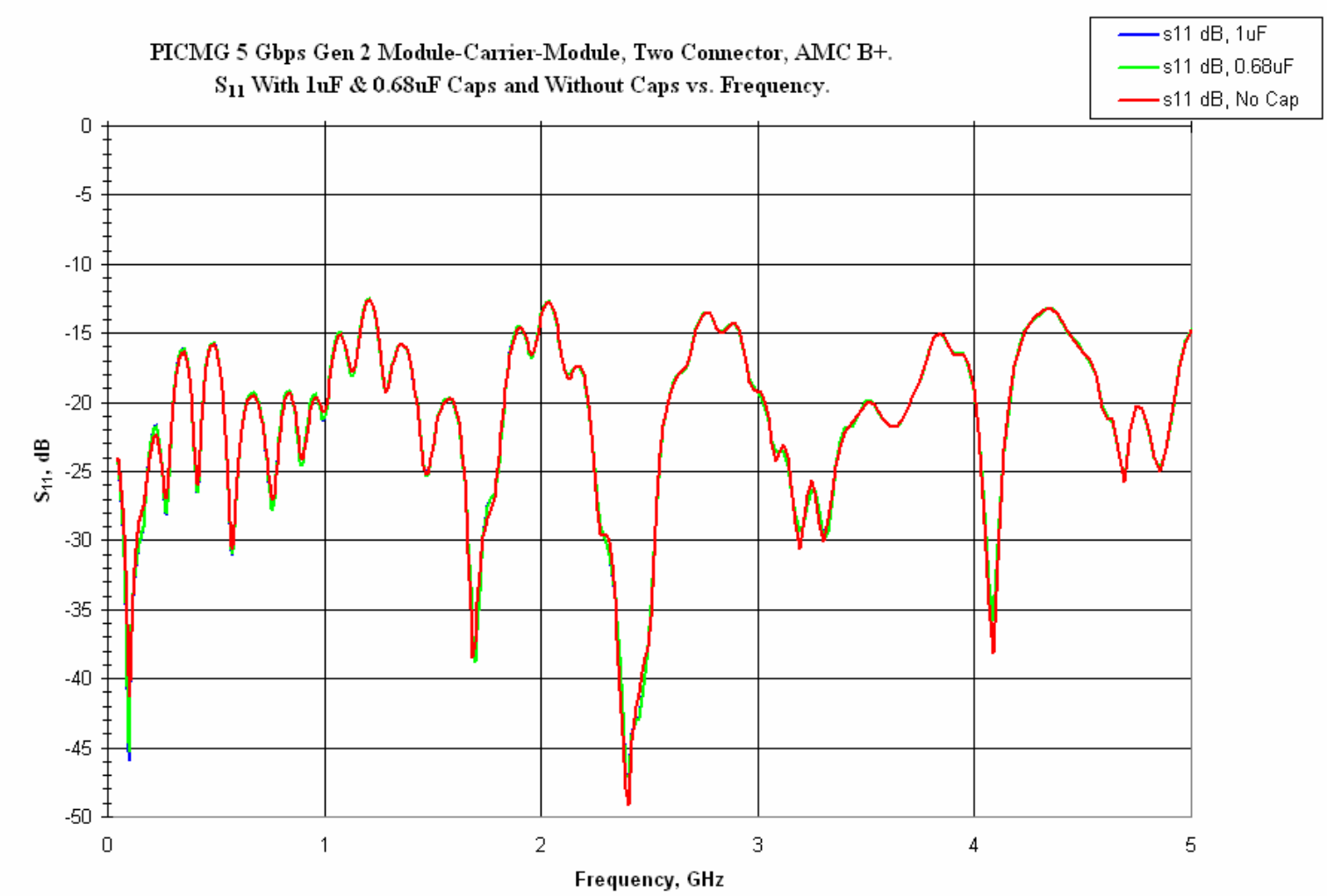

Figure 8: Return loss for module-carrier-module channel with and without caps.

The impulse response of the channel with the 1µF caps is shown in Figure 9 below. The impulse response measures how long energy will continue propagate in the system before it damps out. For the module-carrier-module channel with a 1UI pulse input, note that the energy is significantly damped within 3UI -- which is good. The tail shows the desired smooth response.

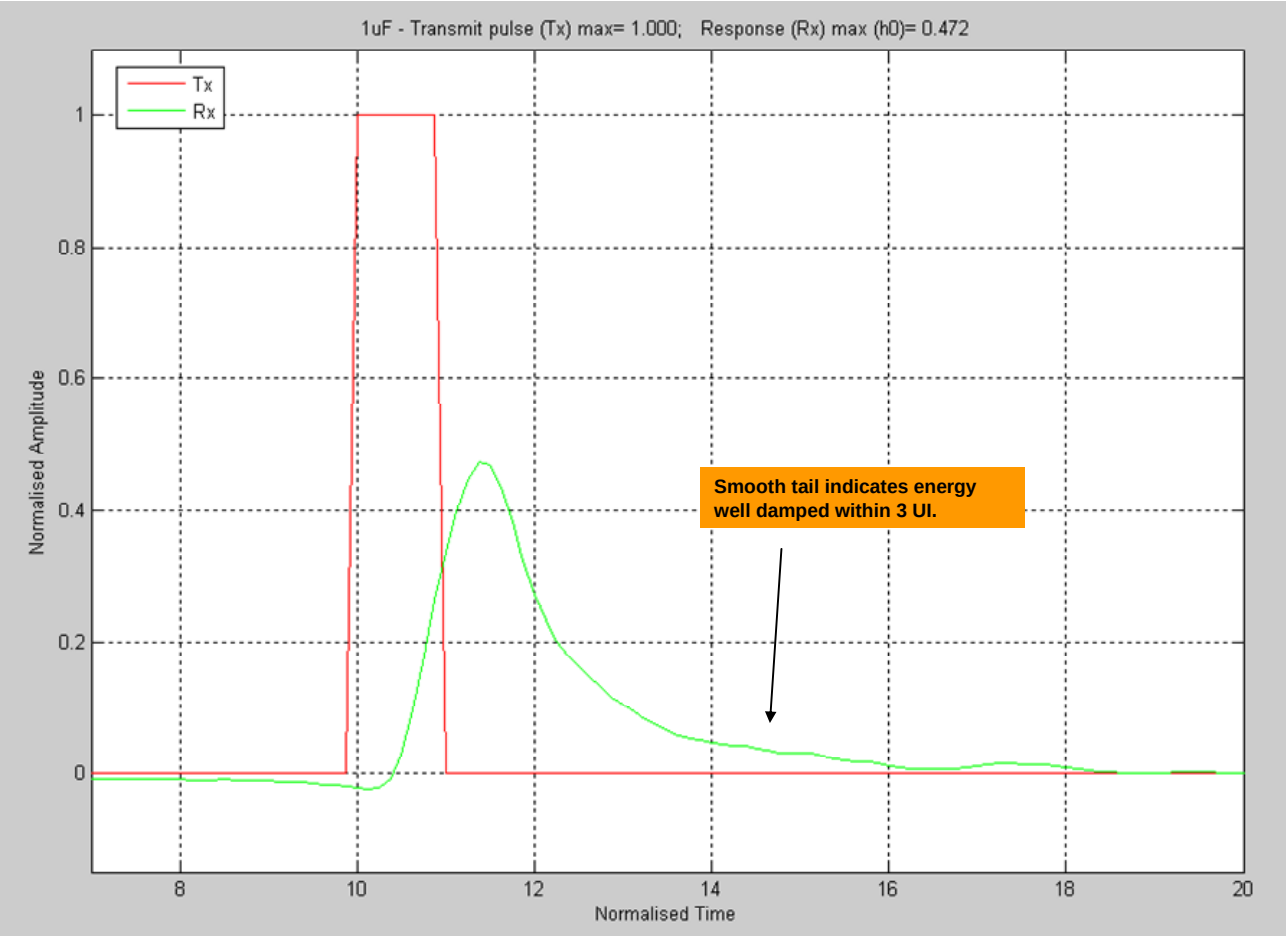

Figure 9: Impulse response with 1µF cap shows energy is well damped.

The impulse response of the link with the 0.68µF caps is shown in Figure 10 below. It looks essentially identical to the 1µF cap.

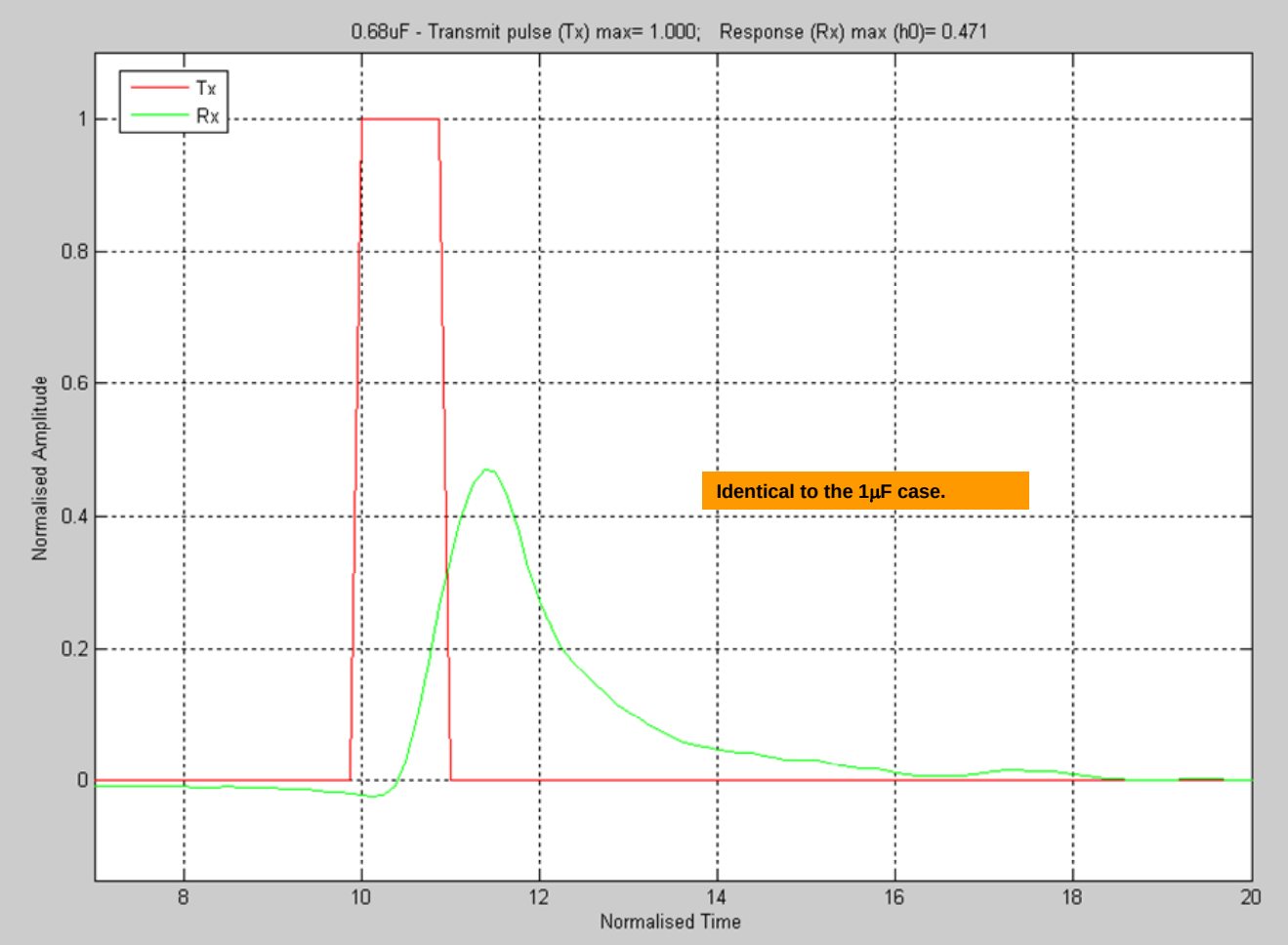

Figure 10: Impulse response with 0.68µF cap is identical to the 1µF cap.

Figure 11 shows the impulse response with the caps removed. It looks essentially the same as with the caps.

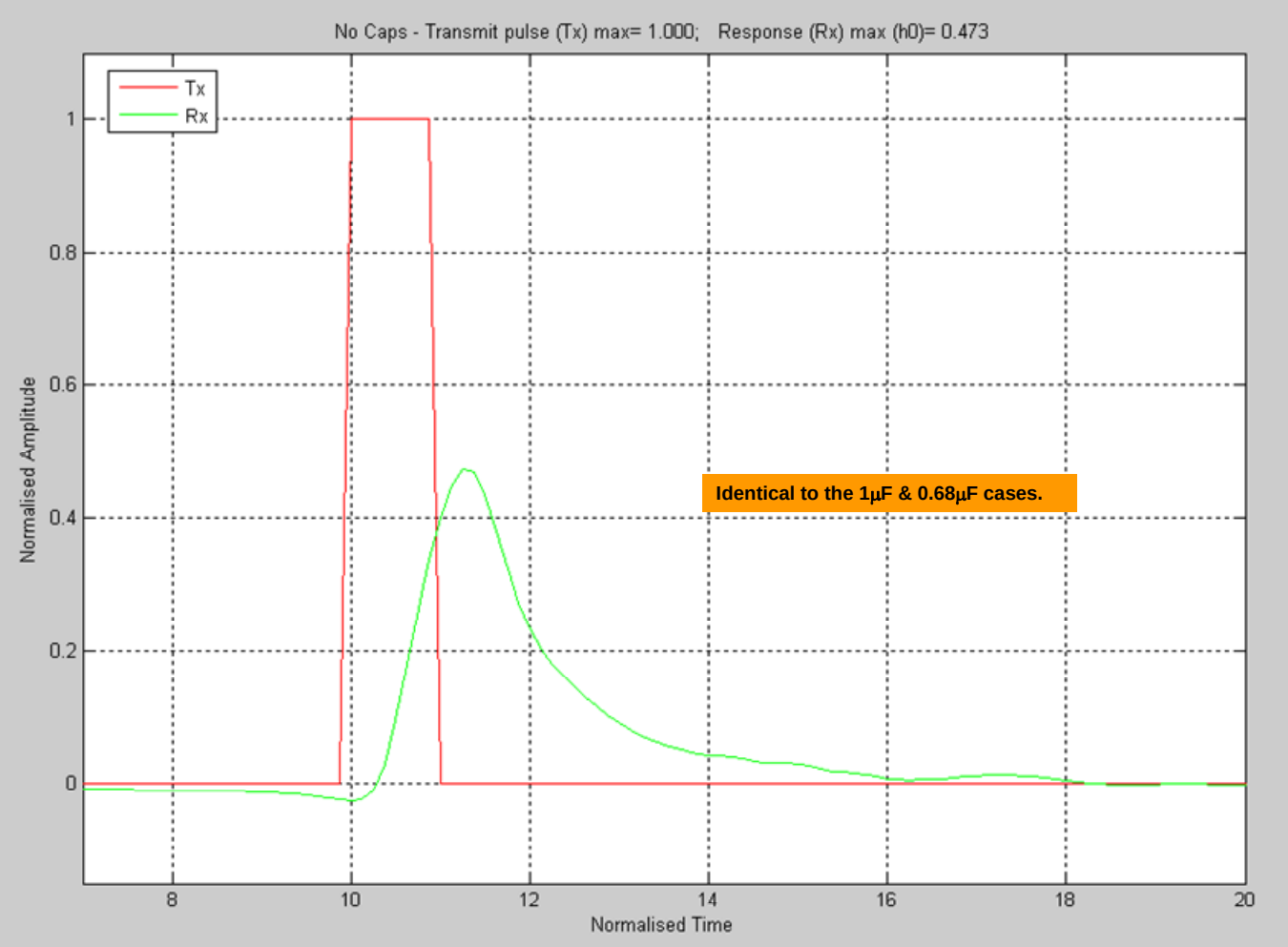

Figure 11: Impulse response without the caps shows no significant differences.